

Product Specification

Part Name:OEL Display Module

Part ID: LYA130WG30-128064

Ver: C

Customer:
Approved by

From: Li Yuan Electronics Co.,Ltd.
Approved by

Notes:

1. Please contact Li Yuan Electronics before assigning your product based on this module specification
2. The information contained herein is presented merely to indicate the characteristics and performance of our products. No responsibility is assumed by Li Yuan Electronics for any intellectual property claims or other problems that may result from application based on the module described herein.



Part Number	Revision	Revision Content	Revised on
LYA130WG30-128064	A	New	20130603
	B	修改 CIE 值	20150108
	C	应用原理图增加特别提醒	20150525

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1. Basic Specifications

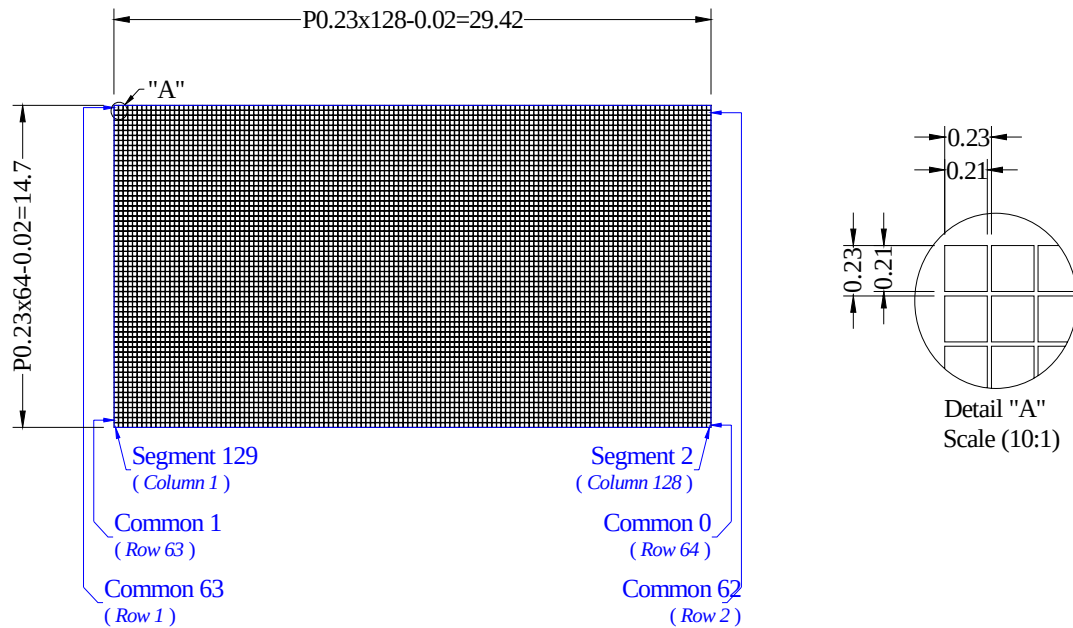
1.1 Display Specifications

- 1) Display Mode: Passive Matrix
- 2) Display Color: Monochrome (White)
- 3) Drive Duty: 1/64 Duty

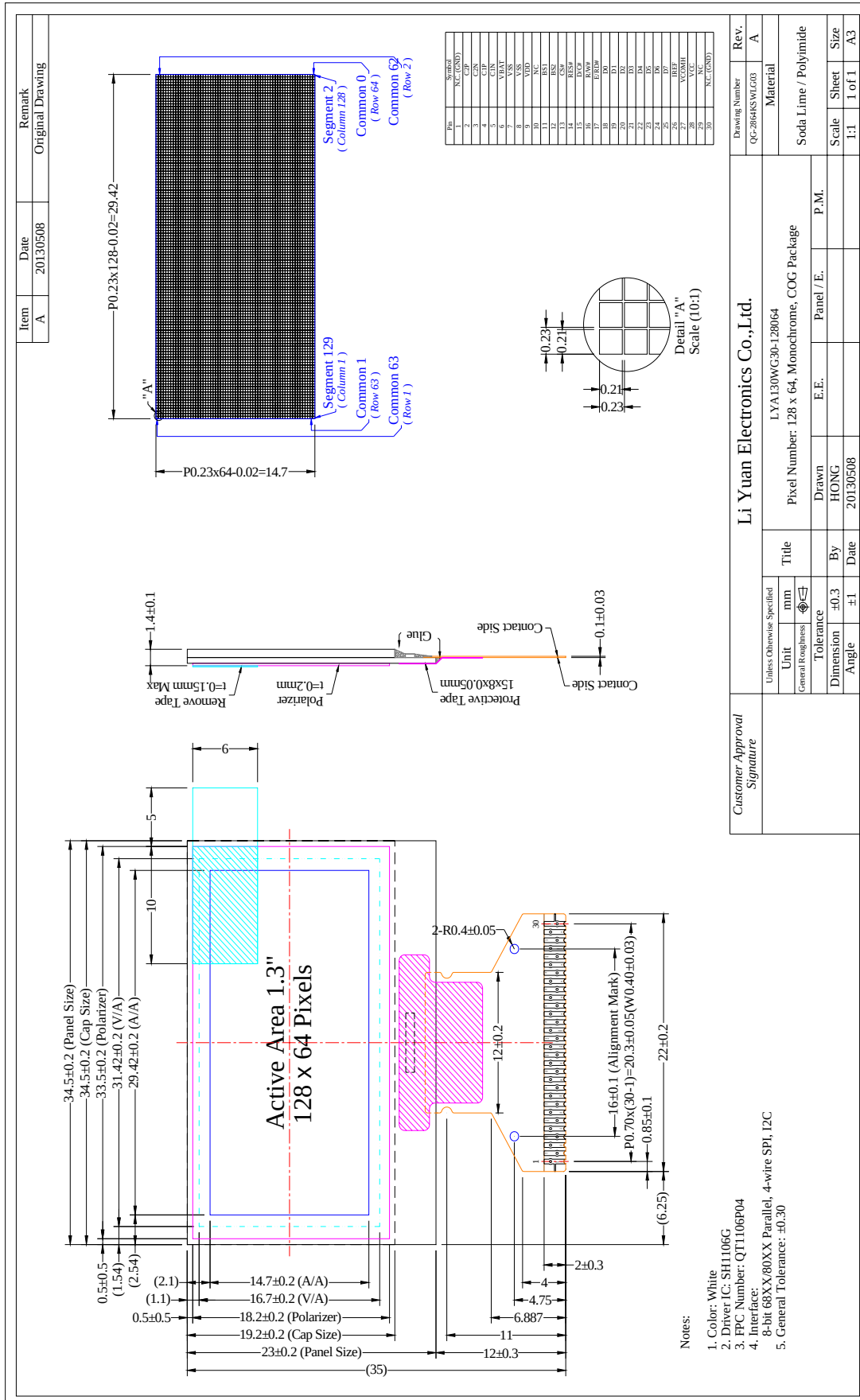
1.2 Mechanical Specifications

- 1) Outline Drawing: According to the annexed outline drawing
- 2) Number of Pixels: 128×64
- 3) Panel Size: $34.5 \times 23.0 \times 1.4$ (mm)
- 4) Active Area: 29.42×14.7 (mm)
- 5) Pixel Pitch: 0.23×0.23 (mm)
- 6) Pixel Size: 0.21×0.21 (mm)
- 7) Weight: 2.18 (g)

1.3 Active Area / Memory Mapping & Pixel Construction



1.4 Mechanical Drawing



1.5 Pin Definition

Pin Number	Symbol	I/O	Function															
Power Supply																		
9	VDD	P	Power Supply for Logic This is a voltage supply pin. It must be connected to external source.															
7、8	VSS	P	Ground of Logic Circuit This is a ground pin. It acts as a reference for the logic pins. It must be connected to external ground.															
28	VCC	P	Power Supply for OEL Panel This is the most positive voltage supply pin of the chip. A stabilization capacitor should be connected between this pin and V _{SS} when the converter is used. It must be connected to external source when the converter is not used.															
1、10、29、30	NC	-																
Driver																		
26	IREF	I	Current Reference for Brightness Adjustment This pin is segment current reference pin. A resistor should be connected between this pin and V _{SS} . Set the current at 12.5μA maximum.															
27	VCOMH	O	Voltage Output High Level for COM Signal This pin is the input pin for the voltage output high level for COM signals. A capacitor should be connected between this pin and V _{SS} .															
DC/DC Converter																		
6	VBAT	P	Power Supply for DC/DC Converter Circuit This is the power supply pin for the internal buffer of the DC/DC voltage converter. This pin should be disconnected when VPP is supplied externally															
4 / 5 2 / 3	C1P / C1N C2P / C2N	I	Positive Terminal of the Flying Inverting Capacitor Negative Terminal of the Flying Boost Capacitor The charge-pump capacitors are required between the terminals. They must be floated when the converter is not used.															
Interface																		
11 12	BS1 BS2	I	Communicating Protocol Select These pins are MCU interface selection input. See the following table: <table><tr><td></td><td>BS1</td><td>BS2</td></tr><tr><td>I²C</td><td>1</td><td>0</td></tr><tr><td>4-wire SPI</td><td>0</td><td>0</td></tr><tr><td>8-bit 68XX Parallel</td><td>0</td><td>1</td></tr><tr><td>8-bit 80XX Parallel</td><td>1</td><td>1</td></tr></table>		BS1	BS2	I ² C	1	0	4-wire SPI	0	0	8-bit 68XX Parallel	0	1	8-bit 80XX Parallel	1	1
	BS1	BS2																
I ² C	1	0																
4-wire SPI	0	0																
8-bit 68XX Parallel	0	1																
8-bit 80XX Parallel	1	1																
14	RES#	I	Power Reset for Controller and Driver This pin is reset signal input. When the pin is low, initialization of the chip is executed. Keep this pin pull high during normal operation.															
13	CS#	I	Chip Select This pin is the chip select input. The chip is enabled for MCU communication only when CS# is pulled low.															
15	D/C#	I	Data/Command Control This pin is Data/Command control pin. When the pin is pulled high, the input at D7~D0 is treated as display data. When the pin is pulled low, the input at D7~D0 will be transferred to the command register. When the pin is pulled high and serial interface mode is selected, the data at SDIN will be interpreted as data. When it is pulled low, the data at SDIN will be transferred to the command register. In I ² C mode, this pin acts as SA0 for slave address selection. For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams.															
17	E/RD#	I	Read/Write Enable or Read This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled high and the CS# is pulled low. When connecting to an 80XX-microprocessor, this pin receives the Read (RD#) signal. Data read operation is initiated when this pin is pulled low and CS# is pulled low. When serial or I ² C mode is selected, this pin must be connected to V _{SS} .															

1.5 Pin Definition (Continued)

Pin Number	Symbol	I/O	Function
Interface (Continued)			
16	R/W#	I	Read/Write Select or Write This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as Read/Write (R/W#) selection input. Pull this pin to "High" for read mode and pull it to "Low" for write mode. When 80XX interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled low and the CS# is pulled low. When serial or I ² C mode is selected, this pin must be connected to V _{SS} .
18~25	D0~D7	I/O	Host Data Input/Output Bus These pins are 8-bit bi-directional data bus to be connected to the microprocessor's data bus. When serial mode is selected, D1 will be the serial data input SDIN and D0 will be the serial clock input SCLK. When I ² C mode is selected, D2 & D1 should be tied together and serve as SDA _{out} & SDA _{in} in application and D0 is the serial clock input SCL. Unused pins must be connected to V _{SS} except for D2 in serial mode.
Reserve			

2. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Notes
Supply Voltage for Logic	V _{DD}	-0.3	4	V	1, 2
Supply Voltage for Display	V _{CC}	0	14	V	1, 2
Supply Voltage for DC/DC	V _{BAT}	-0.3	5	V	1, 2
Operating Temperature	T _{OP}	-40	85	°C	
Storage Temperature	T _{STG}	-40	85	°C	3
Life Time (120 cd/m ²)		10,000	-	hour	4
Life Time (80 cd/m ²)		30,000	-	hour	4
Life Time (60 cd/m ²)		50,000	-	hour	4

Note 1: All the above voltages are on the basis of "V_{SS} = 0V".

Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. Also, for normal operations, it is desirable to use this module under the conditions according to Section 3. "Optics & Electrical Characteristics". If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate.

Note 3: The defined temperature ranges do not include the polarizer. The maximum withstood temperature of the polarizer should be 80°C.

Note 4: V_{CC} = 12.0V, T_a = 25°C, 50% Checkerboard.

Software configuration follows Section 4.4 Initialization.

End of lifetime is specified as 50% of initial brightness reached. The average operating lifetime at room temperature is estimated by the accelerated operation at high temperature conditions.

3. Optics & Electrical Characteristics

3.1 Optics Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Brightness (V _{CC} Supplied Externally)	L _{br}	Note 5	100	-	-	cd/m ²
<i>Brightness (V_{CC} Generated by Internal DC/DC)</i>	<i>L_{br}</i>	<i>Note 6</i>	<i>90</i>	<i>110</i>	<i>130</i>	<i>cd/m²</i>
C.I.E. (White)	(x) (y)	C.I.E. 1931	0.25 0.27	0.29 0.31	0.33 0.35	
Dark Room Contrast	CR		-	2000:1	-	
Viewing Angle			-	Free	-	degree

* Optical measurement taken at V_{DD} = 2.8V, V_{CC} = 12V & 8V.
Software configuration follows Section 4.4 Initialization.

3.2 DC Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage for Logic	V _{DD}		1.65	2.8	3.3	V
Supply Voltage for Display (Supplied Externally)	V _{CC}	Note 5 (Internal DC/DC Disable)	-	12	-	V
<i>Supply Voltage for DC/DC</i>	<i>V_{BAT}</i>	<i>Internal DC/DC Enable</i>	<i>3.5</i>	<i>-</i>	<i>4.2</i>	<i>V</i>
<i>Supply Voltage for Display (Generated by Internal DC/DC)</i>	<i>V_{CC}</i>	<i>Note 6 (Internal DC/DC Enable)</i>	<i>6.4</i>	<i>-</i>	<i>9</i>	<i>V</i>
High Level Input	V _{IH}	I _{OUT} = 100μA, 3.3MHz	0.8×V _{DD}	-	V _{DD}	V
Low Level Input	V _{IL}	I _{OUT} = 100μA, 3.3MHz	0	-	0.2×V _{DD}	V
High Level Output	V _{OH}	I _{OUT} = 100μA, 3.3MHz	0.9×V _{DD}	-	V _{DD}	V
Low Level Output	V _{OL}	I _{OUT} = 100μA, 3.3MHz	0	-	0.1×V _{DD}	V
Operating Current for V _{DD}	I _{DD}		-	180	300	μA
Operating Current for V _{CC} (V _{CC} Supplied Externally)	I _{CC}	Note 7	-	23	32	mA
<i>Operating Current for V_{BAT} (V_{CC} Generated by Internal DC/DC)</i>	<i>I_{BAT}</i>	<i>Note 8</i>	<i>-</i>	<i>45</i>	<i>50</i>	<i>mA</i>
Sleep Mode Current for V _{DD}	I _{DD, SLEEP}		-	1	5	μA
Sleep Mode Current for V _{CC}	I _{CC, SLEEP}		-	2	10	μA

Note 5 & 6: Brightness (L_{br}) and Supply Voltage for Display (V_{CC}) are subject to the change of the panel characteristics and the customer's request.

Note 7: V_{DD} = 2.8V, V_{CC} = 12V, IREF=910K 100% Display Area Turn on.

Note 8: V_{DD} = 2.8V, V_{CC} = 8V, IREF=560K 100% Display Area Turn on.

* Software configuration follows Section 4.4 Initialization.

3.3 AC Characteristics

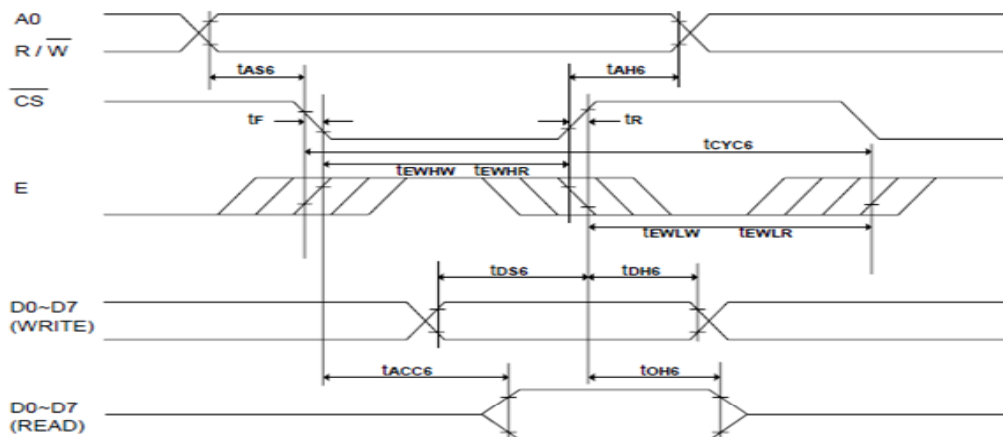
3.3.1.1 68XX-Series MPU Parallel Interface Timing Characteristics:

(V_{DD1} = 1.65 - 3.5V, T_A = +25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t _{CYC6}	System cycle time	600	-	-	ns	
t _{AS6}	Address setup time	0	-	-	ns	
t _{AH6}	Address hold time	0	-	-	ns	
t _{DS6}	Data setup time	80	-	-	ns	
t _{DH6}	Data hold time	30	-	-	ns	
t _{OH6}	Output disable time	20	-	140	ns	C _L = 100pF
t _{ACC6}	Access time	-	-	280	ns	C _L = 100pF
t _{EWHW}	Enable H pulse width (Write)	200	-	-	ns	
t _{EWHR}	Enable H pulse width (Read)	240	-	-	ns	
t _{EWLW}	Enable L pulse width (Write)	200	-	-	ns	
t _{EWLR}	Enable L pulse width (Read)	200	-	-	ns	
t _R	Rise time	-	-	30	ns	
t _F	Fall time	-	-	30	ns	

(V_{DD1} = 2.4 - 3.5V, T_A = +25°C)

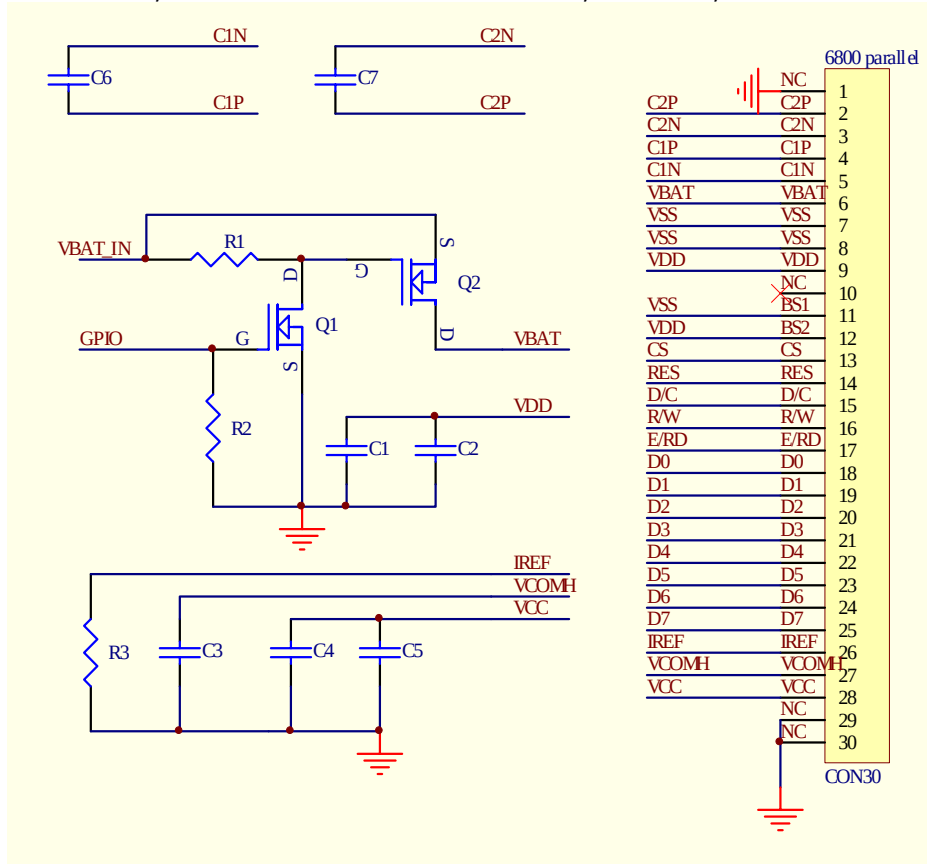
Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t _{CYC6}	System cycle time	300	-	-	ns	
t _{AS6}	Address setup time	0	-	-	ns	
t _{AH6}	Address hold time	0	-	-	ns	
t _{DS6}	Data setup time	40	-	-	ns	
t _{DH6}	Data hold time	15	-	-	ns	
t _{OH6}	Output disable time	10	-	70	ns	C _L = 100pF
t _{ACC6}	Access time	-	-	140	ns	C _L = 100pF
t _{EWHW}	Enable H pulse width (Write)	100	-	-	ns	
t _{EWHR}	Enable H pulse width (Read)	120	-	-	ns	
t _{EWLW}	Enable L pulse width (Write)	100	-	-	ns	
t _{EWLR}	Enable L pulse width (Read)	100	-	-	ns	
t _R	Rise time	-	-	15	ns	
t _F	Fall time	-	-	15	ns	



3.3.1.2 68XX-Series MPU Parallel Interface with Internal Charge Pump

特别提醒(Special Tips): 主板设计务必加电子开关, 否则, 可能引起漏电流现象

(When design main board, Please add Electronic Switch circuit, otherwise, will be caused leak current)



Recommended Components:

- C1, C5: 1μF / 16V, X5R
- C2, C3, C4: 2.2μF / 16V, X5R
- C6, C7: 1μF / 16V, X7R
- R3: 560kΩ, $R3 = (\text{Voltage at IREF} - \text{VSS}) / \text{IREF}$
- R1, R2: 47kΩ
- Q1: FDN338P
- Q2: FDN335N

Notes:

VDD: 1.65~3.3V, it should be equal to MPU I/O voltage.

Vin: 3.5~4.2V

* VBAT will be connected to VDD when VCC be connected to external source (12V), R3 should be replaced as **910 kΩ**.

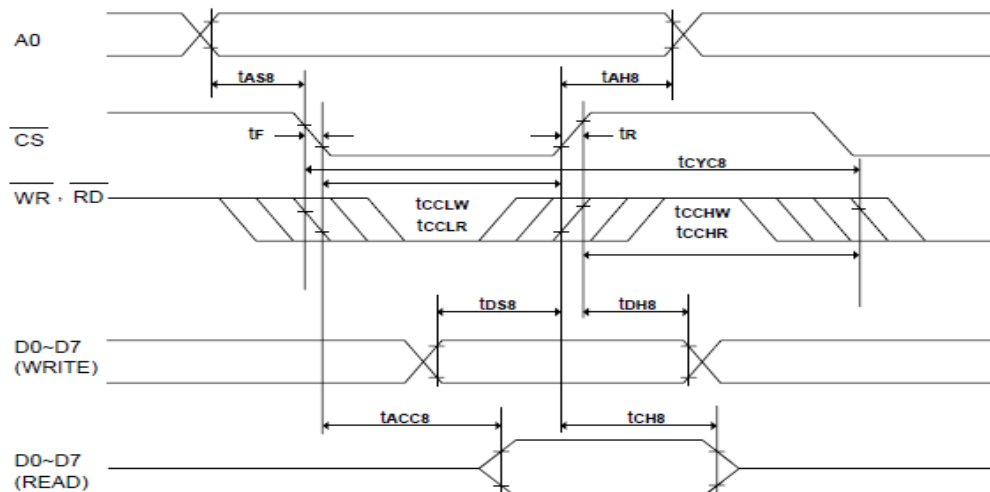
3.3.2.1 80XX-Series MPU Parallel Interface Timing Characteristics:

(VDD1 = 1.65 - 3.5V, TA = +25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
tcyc8	System cycle time	600	-	-	ns	
tas8	Address setup time	0	-	-	ns	
tah8	Address hold time	0	-	-	ns	
tds8	Data setup time	80	-	-	ns	
tdh8	Data hold time	30	-	-	ns	
tch8	Output disable time	20	-	140	ns	CL = 100pF
tacc8	$\overline{RD}$ access time	-	-	280	ns	CL = 100pF
tcclw	Control L pulse width (WR)	200	-	-	ns	
tcclr	Control L pulse width (RD)	240	-	-	ns	
tcchw	Control H pulse width (WR)	200	-	-	ns	
tcchr	Control H pulse width (RD)	200	-	-	ns	
tr	Rise time	-	-	30	ns	
tf	Fall time	-	-	30	ns	

(VDD1 = 2.4 - 3.5V, TA = +25°C)

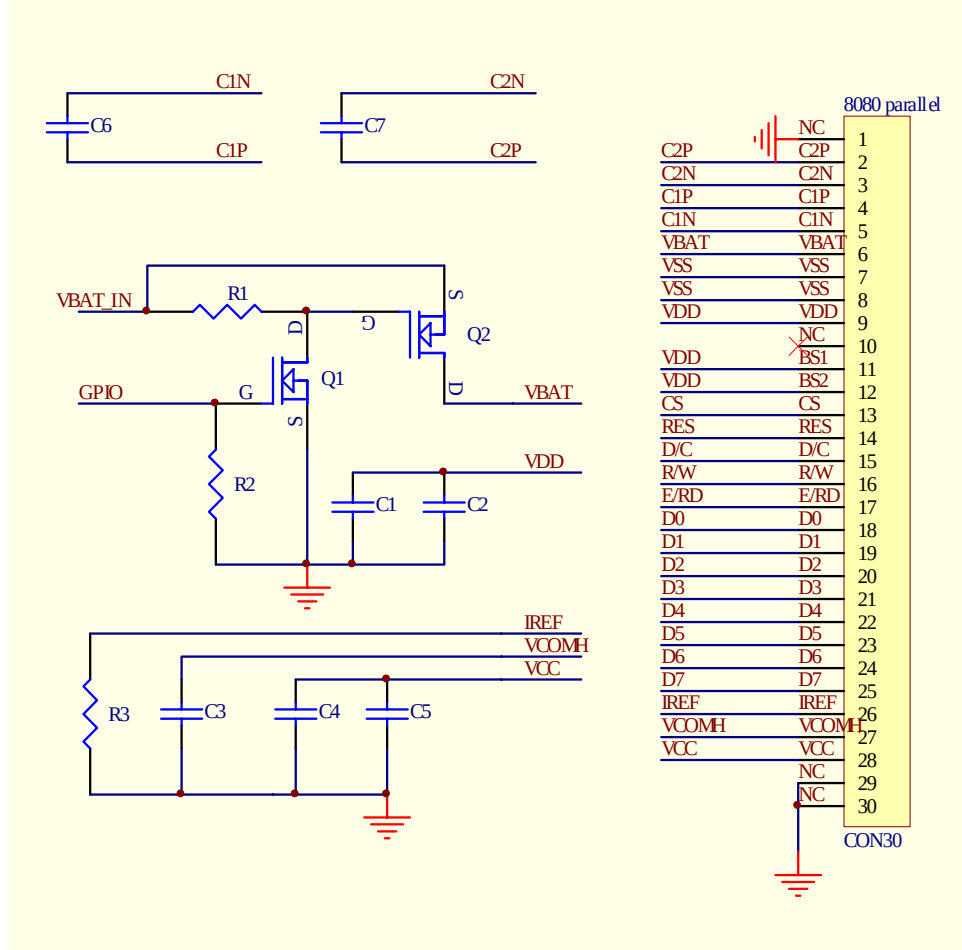
Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
tcyc8	System cycle time	300	-	-	ns	
tas8	Address setup time	0	-	-	ns	
tah8	Address hold time	0	-	-	ns	
tds8	Data setup time	40	-	-	ns	
tdh8	Data hold time	15	-	-	ns	
tch8	Output disable time	10	-	70	ns	CL = 100pF
tacc8	$\overline{RD}$ access time	-	-	140	ns	CL = 100pF
tcclw	Control L pulse width (WR)	100	-	-	ns	
tcclr	Control L pulse width (RD)	120	-	-	ns	
tcchw	Control H pulse width (WR)	100	-	-	ns	
tcchr	Control H pulse width (RD)	100	-	-	ns	
tr	Rise time	-	-	15	ns	
tf	Fall time	-	-	15	ns	



3.3.2.2 80XX-Series MPU Parallel Interface with Internal Charge Pump

特别提醒(Special Tips): 主板设计务必加电子开关, 否则, 可能引起漏电流现象

(When design main board, Please add Electronic Switch circuit, otherwise, will be caused leak current)



Recommended Components:

C1, C5: 1 μ F / 16V, X5R
C2, C3, C4: 2.2 μ F / 16V, X5R
C6, C7: 1 μ F / 16V, X7R
R3: 560k Ω , $R3 = (\text{Voltage at IREF} - VSS) / IREF$
R1, R2: 47k Ω
Q1: FDN338P
Q2: FDN335N

Notes:

VDD: 1.65~3.3V, it should be equal to MPU I/O voltage.

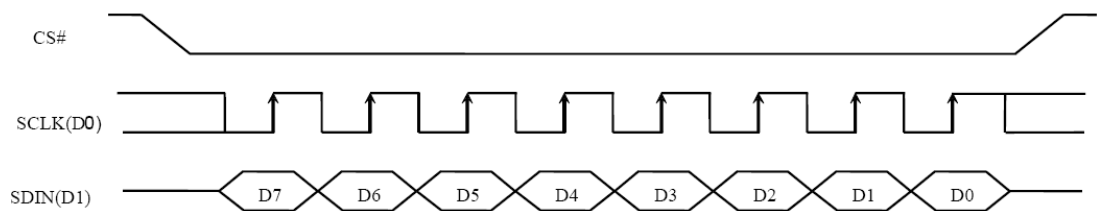
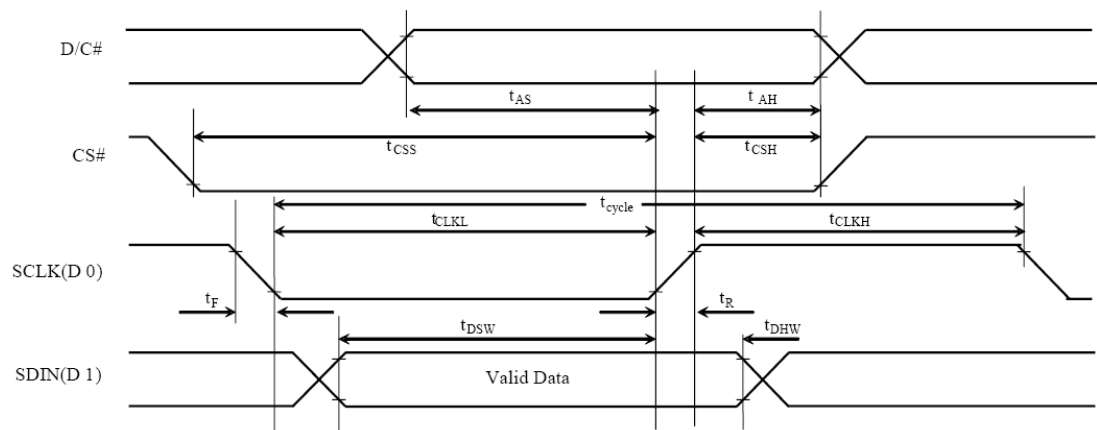
Vin: 3.5~4.2V

* VBAT will be connected to VDD when VCC be connected to external source (12V), R3 should be replaced as **910 k Ω** .

3.3.3.1 Serial Interface Timing Characteristics: (4-wire SPI)

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	ns
t_{AS}	Address Setup Time	15	-	ns
t_{AH}	Address Hold Time	15	-	ns
t_{CSS}	Chip Select Setup Time	20	-	ns
t_{CSH}	Chip Select Hold Time	10	-	ns
t_{DSW}	Write Data Setup Time	15	-	ns
t_{DHW}	Write Data Hold Time	15	-	ns
t_{CLKL}	Clock Low Time	20	-	ns
t_{CLKH}	Clock High Time	20	-	ns
t_{R}	Rise Time	-	40	ns
t_{F}	Fall Time	-	40	ns

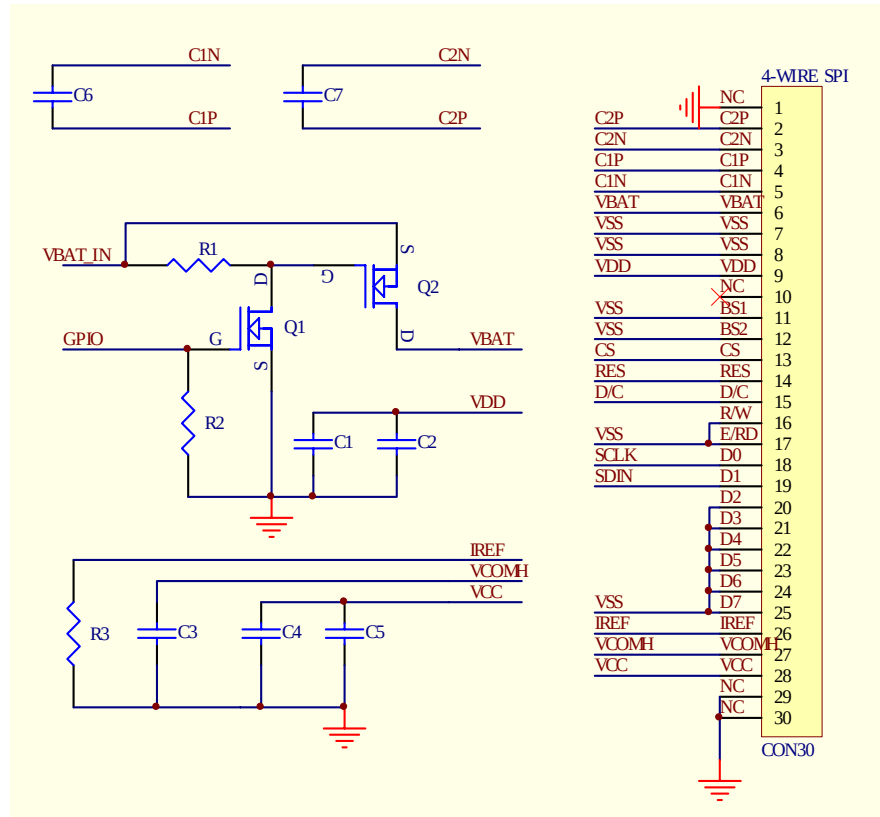
* ($V_{\text{DD}} - V_{\text{SS}} = 1.65\text{V to } 3.3\text{V}$, $T_a = 25^\circ\text{C}$)



3.3.3.2 4-wire Serial Interface with Internal Charge Pump

特别提醒(Special Tips): 主板设计务必加电子开关, 否则, 可能引起漏电流现象

(When design main board, Please add Electronic Switch circuit, otherwise, will be caused leak current)



Recommended Components:

C1, C5: 1 μ F / 16V, X5R
 C2, C3, C4: 2.2 μ F / 16V, X5R
 C6, C7: 1 μ F / 16V, X7R
 R3: 560k Ω , R3 = (Voltage at IREF - VSS) / IREF
 R1, R2: 47k Ω
 Q1: FDN338P
 Q2: FDN335N

Notes:

VDD: 1.65~3.3V, it should be equal to MPU I/O voltage.

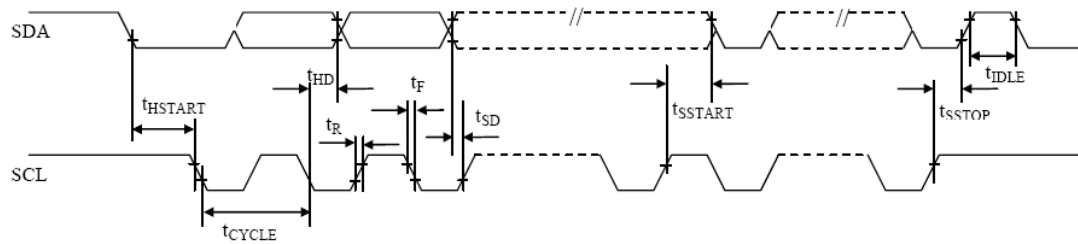
VBAT_in: 3.5~4.2V

* VBAT will be connected to VDD when VCC be connected to external source (12V), R3 should be replaced as **910 k Ω** .

3.3.4.1 I²C Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	2.5	-	μs
t_{HSTART}	Start Condition Hold Time	0.6	-	μs
t_{HD}	Data Hold Time (for "SDA _{OUT} " Pin)	0	-	ns
	Data Hold Time (for "SDA _{IN} " Pin)	300		
t_{SD}	Data Setup Time	100	-	ns
t_{SSTART}	Start Condition Setup Time (Only relevant for a repeated Start condition)	0.6	-	μs
t_{SSTOP}	Stop Condition Setup Time	0.6	-	μs
t_{R}	Rise Time for Data and Clock Pin		300	ns
t_{F}	Fall Time for Data and Clock Pin		300	ns
t_{IDLE}	Idle Time before a New Transmission can Start	1.3	-	μs

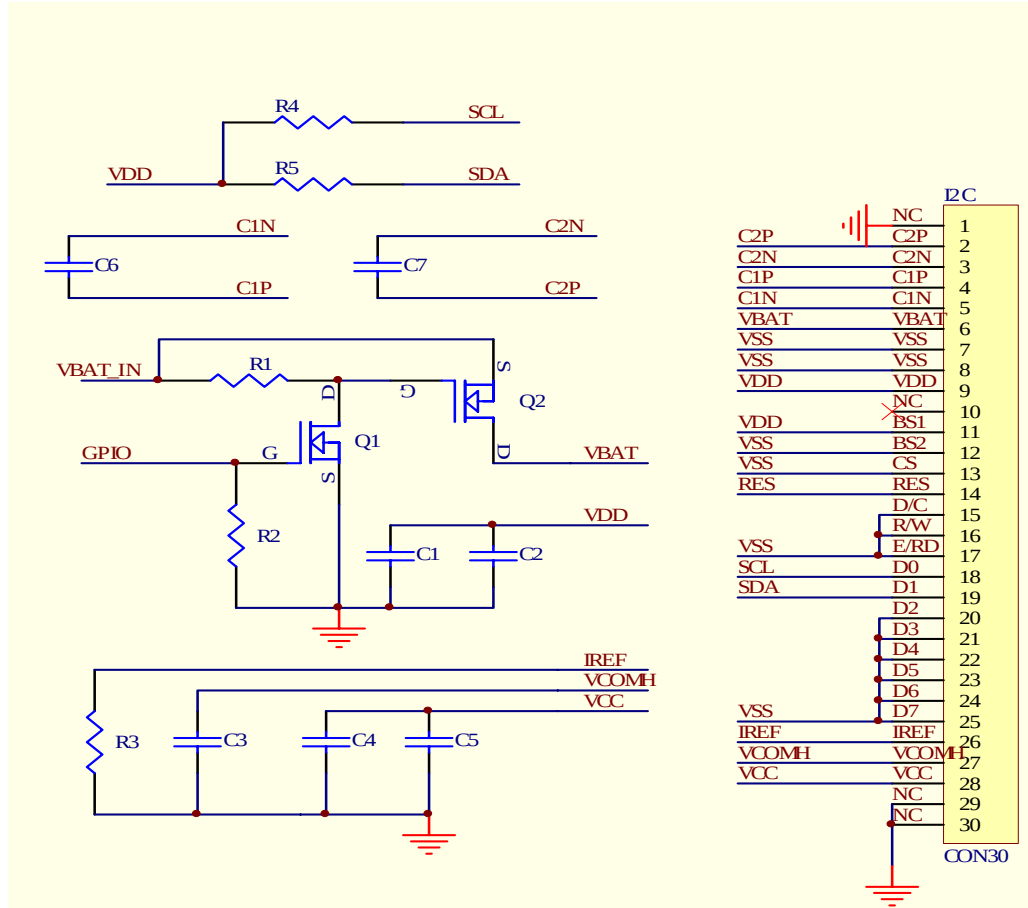
* ($V_{\text{DD}} - V_{\text{SS}} = 1.65\text{V to } 3.3\text{V}$, $T_{\text{a}} = 25^{\circ}\text{C}$)



3.3.5.2 I²C Interface with Internal Charge Pump

特别提醒(Special Tips): 主板设计务必加电子开关, 否则, 可能引起漏电流现象

(When design main board, Please add Electronic Switch circuit, otherwise, will be caused leak current)



Recommended Components:

C1, C5: 1μF / 16V, X5R
C2, C3, C4: 2.2μF / 16V, X5R
C6, C7: 1μF / 16V, X7R
R3: 560kΩ, $R3 = (\text{Voltage at IREF} - VSS) / IREF$
R1, R2: 47kΩ
Q1: FDN338P
Q2: FDN335N

Notes:

VDD: 1.65~3.3V, it should be equal to MPU I/O voltage.

VBAT_in: 3.5~4.2V

* VBAT will be connected to VDD when VCC be connected to external source (12V), R3 should be replaced as **910 kΩ**.

The I²C slave address is 0111100b'. If the customer ties D/C# (pin 15) to VDD, the I²C slave address will be 0111101b'.

4. Functional Specification

4.1 Commands

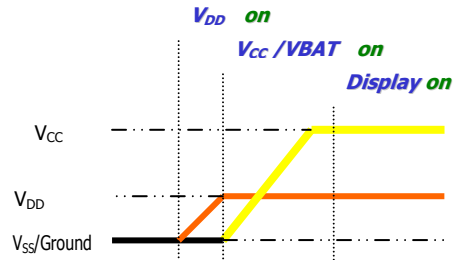
Refer to the Technical Manual for the SH1106

4.2 Power down and Power up Sequence

To protect OEL panel and extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. It gives the OEL panel enough time to complete the action of charge and discharge before/after the operation.

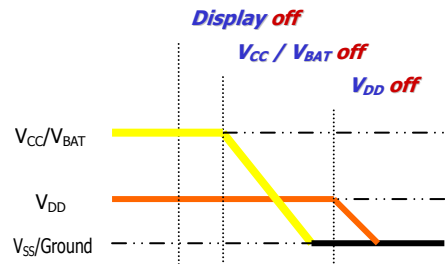
4.2.1 Power up Sequence:

1. Power up V_{DD}
2. Send Display off command
3. Initialization
4. Clear Screen
5. Power up V_{CC}/V_{BAT}
6. Delay 100ms
(When V_{CC} is stable)
7. Send Display on command



4.2.2 Power down Sequence:

1. Send Display off command
2. Power down V_{CC}/V_{BAT}
3. Delay 100ms
(When V_{CC}/V_{BAT} is reach 0 and panel is completely discharges)
4. Power down V_{DD}



Note 13:

- 1) Since an ESD protection circuit is connected between V_{DD} and V_{CC} inside the driver IC, V_{CC} becomes lower than V_{DD} whenever V_{DD} is ON and V_{CC} is OFF.
- 2) V_{CC}/V_{BAT} should be kept float (disable) when it is OFF.
- 3) Power Pins (V_{DD} , V_{CC} , V_{BAT}) can never be pulled to ground under any circumstance.
- 4) V_{DD} should not be power down before V_{CC}/V_{BAT} power down.

4.3 Reset Circuit

When RES# input is low, the chip is initialized with the following status:

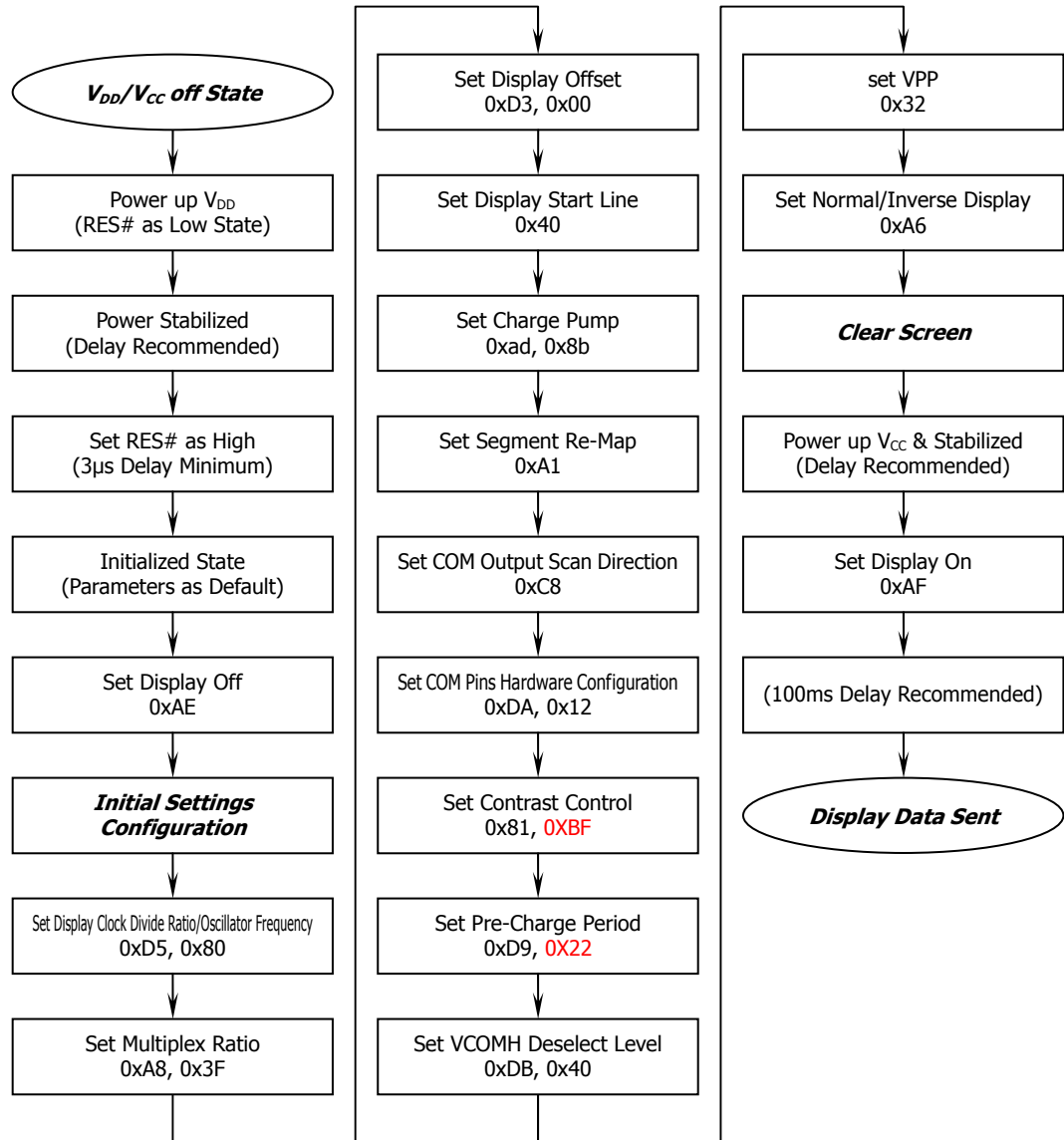
1. Display is OFF
2. 128×64 Display Mode
3. Normal segment and display data column and row address mapping (SEG0 mapped to column address 00h and COM0 mapped to row address 00h)
4. Shift register data clear in serial interface
5. Display start line is set at display RAM address 0
6. Column address counter is set at 0
7. Normal scan direction of the COM outputs
8. Contrast control register is set at 7Fh
9. Normal display mode (Equivalent to A4h command)

4.4 Actual Application Example

Command usage and explanation of an actual example

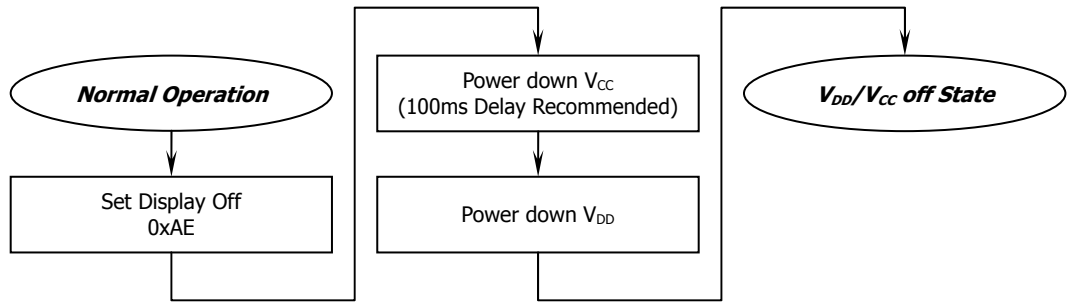
4.4.1 V_{CC} Supplied Externally

<Power up Sequence>

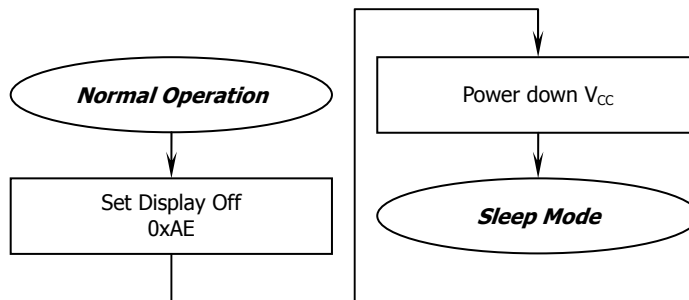


If the noise is accidentally occurred at the displaying window during the operation, please reset the display in order to recover the display function.

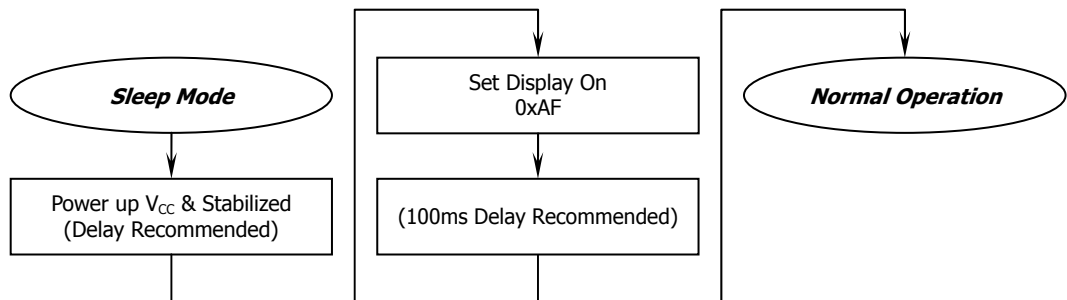
<Power down Sequence>



<Entering Sleep Mode>



<Exiting Sleep Mode>



External setting

```

{
    RES=1;
    delay(1000);
    RES=0;
    delay(1000);
    RES=1;
    delay(1000);
    write_i(0xAE);    /*display off*/

    write_i(0x02);    /*set lower column address*/
    write_i(0x10);    /*set higher column address*/

    write_i(0x40);    /*set display start line*/

    write_i(0xB0);    /*set page address*/
  
```

```
write_i(0x81);    /*contract control*/
write_i(0xBF);    /*128*/

write_i(0xA1);    /*set segment remap*/

write_i(0xA6);    /*normal / reverse*/

write_i(0xA8);    /*multiplex ratio*/
write_i(0x3F);    /*duty = 1/64*/

write_i(0xad);    /*set charge pump enable*/
write_i(0x8a);    /*    0x8a    外供 VCC    */

    write_i(0x32);    /*0X30---0X33 set VPP    8V */

write_i(0xC8);    /*Com scan direction*/

write_i(0xD3);    /*set display offset*/
write_i(0x00);    /*    0x20    */

write_i(0xD5);    /*set osc division*/
write_i(0x80);

write_i(0xD9);    /*set pre-charge period*/
write_i(0x22);    /*0x22*/

write_i(0xDA);    /*set COM pins*/
write_i(0x12);

    write_i(0xdb);    /*set vcomh*/
write_i(0x40);

write_i(0xAF);    /*display ON*/
}
```

```
void write_i(unsigned char ins)
{
```

```
    DC=0;
    CS=0;
    WR=1;
    P1=ins;    /*inst*/
    WR=0;
    WR=1;
    CS=1;
```

```
}
```

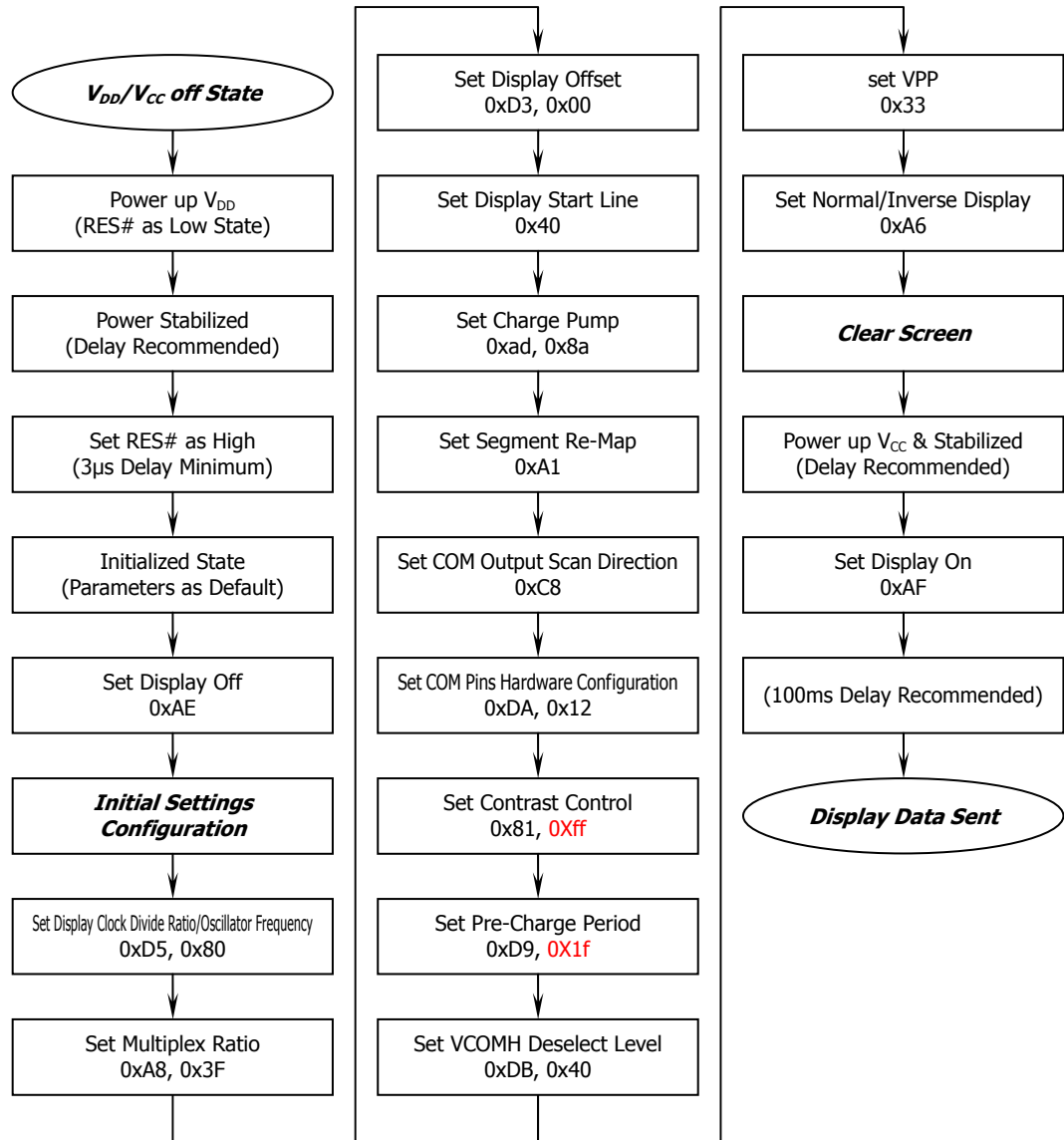
```
void write_d(unsigned char dat)
```

```
{  
    DC=1;  
    CS=0;  
    WR=1;  
    P1=dat;      /*data*/  
    WR=0;  
    WR=1;  
    CS=1;  
}
```

```
void delay(unsigned int i)  
{  
    while(i>0)  
    {  
        i--;  
    }  
}
```

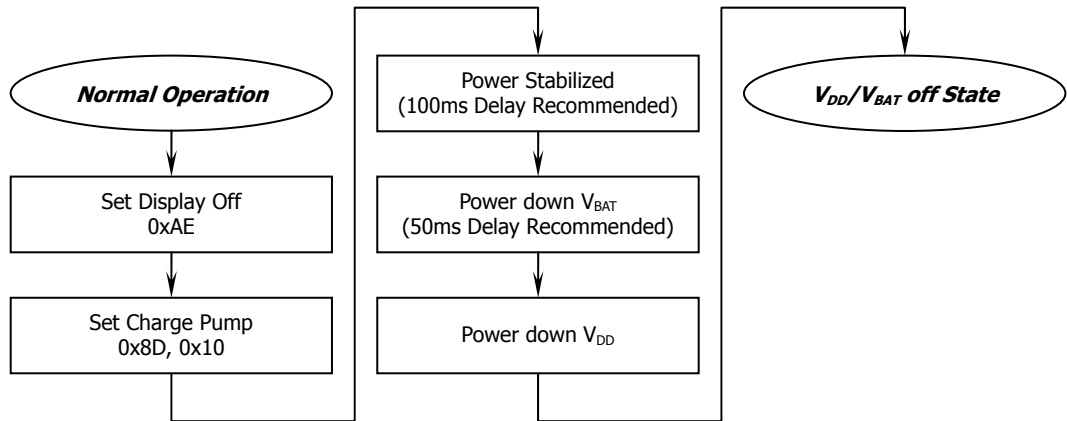
4.4.2 V_{CC} Generated by Internal DC/DC Circuit

<Power up Sequence>

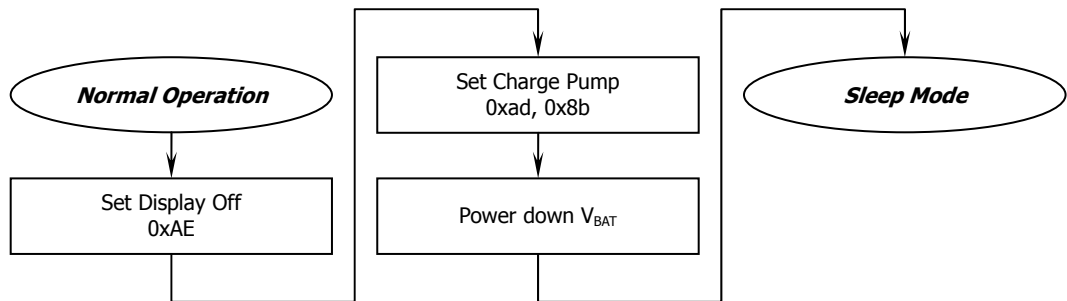


If the noise is accidentally occurred at the displaying window during the operation, please reset the display in order to recover the display function.

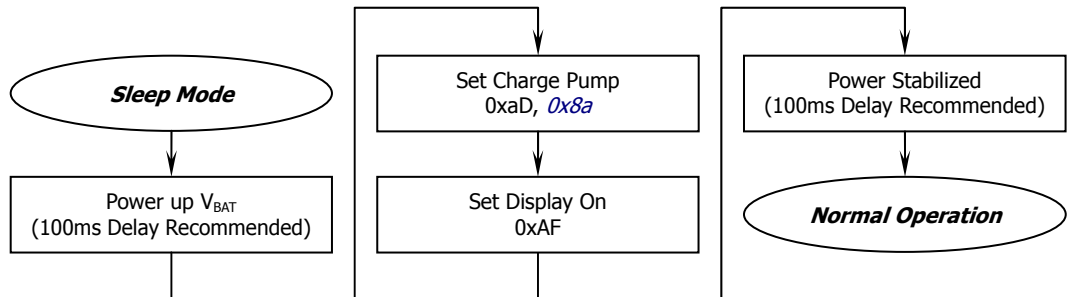
<Power down Sequence>



<Entering Sleep Mode>



<Exiting Sleep Mode>



Internal setting (Charge pump)

```

{
    RES=1;
    delay(1000);
    RES=0;
    delay(1000);
    RES=1;
    delay(1000);
    write_i(0xAE); /*display off*/

```

```

    write_i(0x02); /*set lower column address*/
    write_i(0x10); /*set higher column address*/

```

```
write_i(0x40);    /*set display start line*/

write_i(0xB0);    /*set page address*/

write_i(0x81);    /*contract control*/
write_i(0xff);    /*128*/

write_i(0xA1);    /*set segment remap*/

write_i(0xA6);    /*normal / reverse*/

write_i(0xA8);    /*multiplex ratio*/
write_i(0x3F);    /*duty = 1/64*/

write_i(0xad);    /*set charge pump enable*/
write_i(0x8b);    /*    0x8a    外供 VCC    */

    write_i(0x33);    /*0X30---0X33    set VPP    8V */

write_i(0xC8);    /*Com scan direction*/

write_i(0xD3);    /*set display offset*/
write_i(0x00);    /*    0x20    */

write_i(0xD5);    /*set osc division*/
write_i(0x80);

write_i(0xD9);    /*set pre-charge period*/
write_i(0x1f);    /*0x22*/

write_i(0xDA);    /*set COM pins*/
write_i(0x12);

write_i(0xdb);    /*set vcomh*/
write_i(0x40);

write_i(0xAF);    /*display ON*/
}
```

```
void write_i(unsigned char ins)
{
```

```
    DC=0;
    CS=0;
    WR=1;
    P1=ins;    /*inst*/
    WR=0;
```

```
WR=1;
CS=1;
}

void write_d(unsigned char dat)
{
    DC=1;
    CS=0;
    WR=1;
    P1=dat;      /*data*/
    WR=0;
    WR=1;
    CS=1;
}

void delay(unsigned int i)
{
    while(i>0)
    {
        i--;
    }
}
```

5. Reliability

5.1 Contents of Reliability Tests

Item	Conditions	Criteria
High Temperature Operation	70°C, 240 hrs	The operational functions work.
Low Temperature Operation	-40°C, 240 hrs	
High Temperature Storage	85°C, 240 hrs	
Low Temperature Storage	-40°C, 240 hrs	
High Temperature/Humidity Operation	60°C, 90% RH, 120 hrs	
Thermal Shock	-40°C ⇔ 85°C, 24 cycles 60 mins dwell	

- * The samples used for the above tests do not include polarizer.
- * No moisture condensation is observed during tests.

5.2 Failure Check Standard

After the completion of the described reliability test, the samples were left at room temperature for 2 hrs prior to conducting the failure test at 23±5°C; 55±15% RH.

6. Outgoing Quality Control Specifications

6.1 Environment Required

Customer's test & measurement are required to be conducted under the following conditions:

Temperature:	$23 \pm 5^{\circ}\text{C}$
Humidity:	$55 \pm 15\% \text{ RH}$
Fluorescent Lamp:	30W
Distance between the Panel & Lamp:	$\geq 50\text{cm}$
Distance between the Panel & Eyes of the Inspector:	$\geq 30\text{cm}$
Finger glove (or finger cover) must be worn by the inspector.	
Inspection table or jig must be anti-electrostatic.	

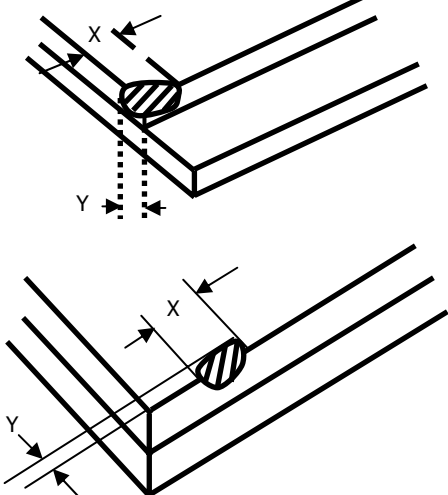
6.2 Sampling Plan

Level II, Normal Inspection, Single Sampling, MIL-STD-105E

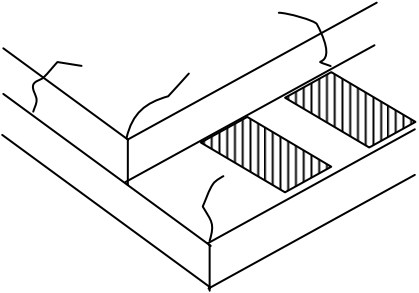
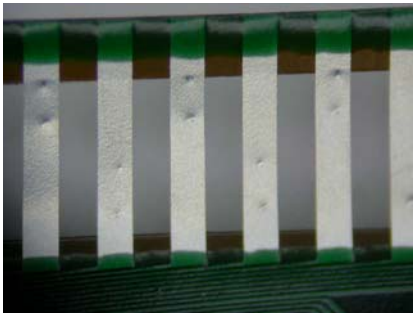
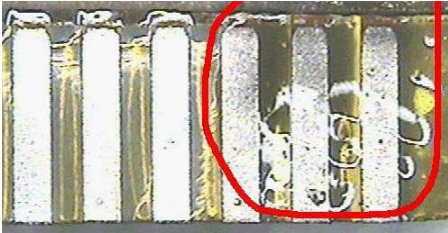
6.3 Criteria & Acceptable Quality Level

Partition	AQL	Definition
Major	0.65	Defects in Pattern Check (Display On)
Minor	1.0	Defects in Cosmetic Check (Display Off)

6.3.1 Cosmetic Check (Display Off) in Non-Active Area

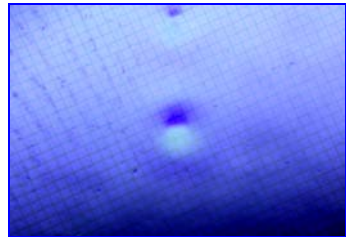
Check Item	Classification	Criteria
Panel General Chipping	Minor	$X > 6 \text{ mm}$ (Along with Edge) $Y > 1 \text{ mm}$ (Perpendicular to edge) 

6.3.1 Cosmetic Check (Display Off) in Non-Active Area (Continued)

Check Item	Classification	Criteria
Panel Crack	Minor	Any crack is not allowable. 
Copper Exposed (Even Pin or Film)	Minor	Not Allowable by Naked Eye Inspection
Film or Trace Damage	Minor	
Terminal Lead Prober Mark	Acceptable	
Glue or Contamination on Pin (Couldn't Be Removed by Alcohol)	Minor	
Ink Marking on Back Side of panel (Exclude on Film)	Acceptable	Ignore for Any

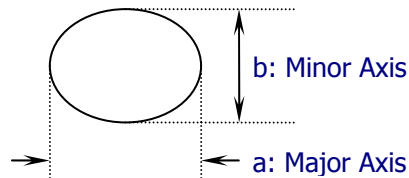
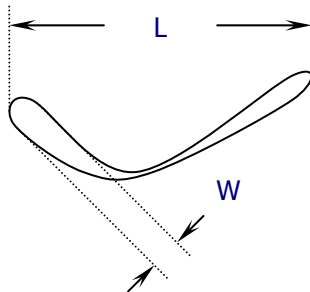
6.3.2 Cosmetic Check (Display Off) in Active Area

It is recommended to execute in clear room environment (class 10k) if actual in necessary.

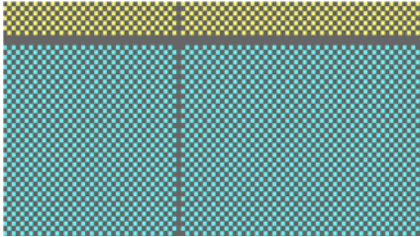
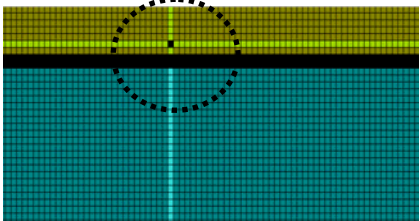
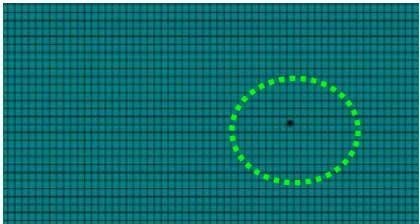
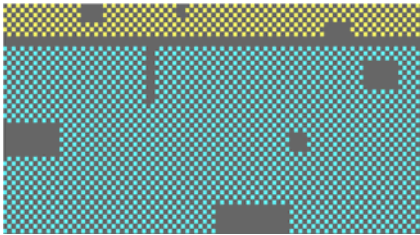
Check Item	Classification	Criteria
Any Dirt & Scratch on Polarizer's Protective Film	Acceptable	Ignore for not Affect the Polarizer
Scratches, Fiber, Line-Shape Defect (On Polarizer)	Minor	$W \leq 0.1$ Ignore $W > 0.1$ $L \leq 2$ $n \leq 1$ $L > 2$ $n = 0$
Dirt, Black Spot, Foreign Material, (On Polarizer)	Minor	$\Phi \leq 0.1$ Ignore $0.1 < \Phi \leq 0.25$ $n \leq 1$ $0.25 < \Phi$ $n = 0$
Dent, Bubbles, White spot (Any Transparent Spot on Polarizer)	Minor	$\Phi \leq 0.5$ → Ignore if no Influence on Display $0.5 < \Phi$ $n = 0$ 
Fingerprint, Flow Mark (On Polarizer)	Minor	Not Allowable

* Protective film should not be tear off when cosmetic check.

** Definition of W & L & Φ (Unit: mm): $\Phi = (a + b) / 2$



6.3.3 Pattern Check (Display On) in Active Area

Check Item	Classification	Criteria
No Display	Major	
Missing Line	Major	
Pixel Short	Major	
Darker Pixel	Major	
Wrong Display	Major	
Un-uniform	Major	