



PIC18F87J90 Family Data Sheet

**64/80-Pin, High-Performance
Microcontrollers with LCD Driver
and nanoWatt Technology**

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PIC18F87J90 FAMILY

64/80-Pin, High-Performance Microcontrollers with LCD Driver and nanoWatt Technology

LCD Driver and Keypad Interface

Features:

- Direct LCD Panel Drive Capability:
 - Can drive LCD panel while in Sleep mode
- Up to 48 Segments and 192 Pixels, Software Selectable
- Programmable LCD Timing module:
 - Multiple LCD timing sources available
 - Up to four commons: static, 1/2, 1/3 or 1/4 multiplex
 - Static, 1/2 or 1/3 bias configuration
- On-Chip LCD Boost Voltage Regulator for Contrast Control
- Charge Time Measurement Unit (CTMU) for Capacitive Touch Sensing
- ADC for Resistive Touch Sensing

Low-Power Features:

- Power-Managed modes:
 - Run: CPU On, Peripherals On
 - Idle: CPU Off, Peripherals On
 - Sleep: CPU Off, Peripherals Off
- Two-Speed Oscillator Start-up

Flexible Oscillator Structure:

- Two Crystal modes, 4-25 MHz
- Two External Clock modes, up to 48 MHz
- 4x Phase Lock Loop (PLL)
- Internal Oscillator Block with PLL:
 - Eight user-selectable frequencies from 31.25 kHz to 8 MHz
- Secondary Oscillator using Timer1 at 32 kHz
- Fail-Safe Clock Monitor:
 - Allows for safe shutdown if peripheral clock fails

Peripheral Highlights:

- High-Current Sink/Source 25 mA/25 mA (PORTB and PORTC)
- Up to Four External Interrupts
- Four 8-Bit/16-Bit Timer/Counter modules
- Two Capture/Compare/PWM (CCP) modules
- Master Synchronous Serial Port (MSSP) module with Two Modes of Operation:
 - 3-Wire/4-Wire SPI (supports all four SPI modes)
 - I²C™ Master and Slave mode
- One Addressable USART module
- One Enhanced Addressable USART module:
 - LIN/L2802 support
 - Auto-wake-up on Start bit and Break character
 - Auto-Baud Detect (ABD)
- 10-Bit, up to 12-Channel A/D Converter:
 - Auto-acquisition
 - Conversion available during Sleep
- Two Analog Comparators
- Programmable Reference Voltage for Comparators
- Hardware Real-Time Clock and Calendar (RTCC) with Clock, Calendar and Alarm Functions
- Charge Time Measurement Unit (CTMU):
 - Capacitance measurement
 - Time measurement with 1 ns typical resolution

Special Microcontroller Features:

- 10,000 Erase/Write Cycle Flash Program Memory, Typical
- Flash Retention 20 Years, Minimum
- Self-Programmable under Software Control
- Word Write Capability for Flash Program Memory for Data EEPROM Emulators

Device	Flash Program Memory (Bytes)	SRAM Data Memory (Bytes)	I/O	LCD (Pixels)	Timers 8-Bit/16-Bit	CCP	MSSP		USART AUSART	10-Bit A/D (Channels)	Comparators	BOR/LVD	RTCC	CTMU
							SPI	Master I ² C™						
PIC18F66J90	64K	3,923	51	132	1/3	2	Yes	Yes	1/1	12	2	Yes	Yes	Yes
PIC18F67J90	128K	3,923	51	132	1/3	2	Yes	Yes	1/1	12	2	Yes	Yes	Yes
PIC18F86J90	64K	3,923	67	192	1/3	2	Yes	Yes	1/1	12	2	Yes	Yes	Yes
PIC18F87J90	128K	3,923	67	192	1/3	2	Yes	Yes	1/1	12	2	Yes	Yes	Yes

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Special Microcontroller Features (Continued):

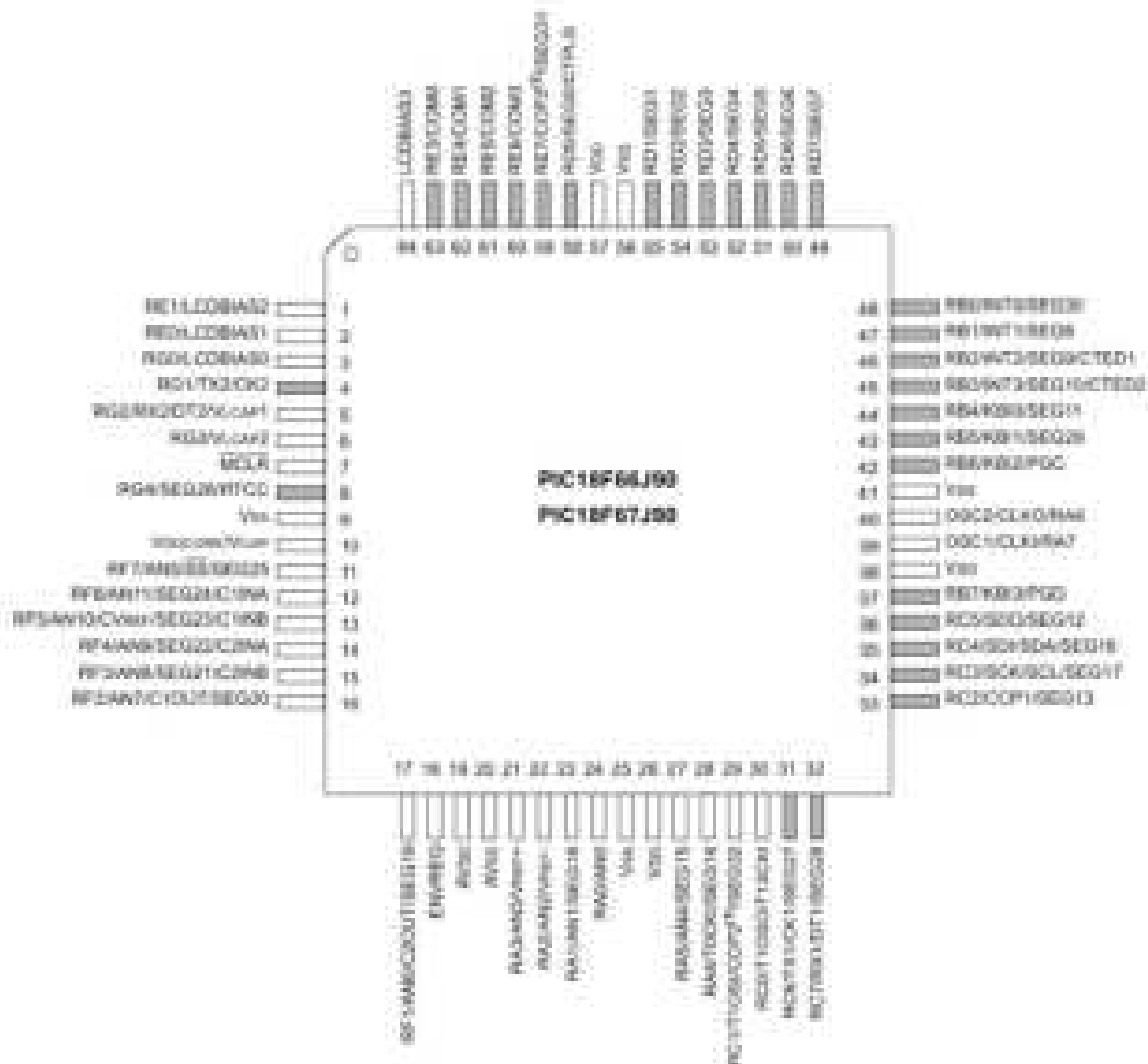
- Priority Levels for interrupts
- 8 × 8 Single-Cycle Hardware Multiplier
- Extended Watchdog Timer (WDT):
 - Programmable period from 4 ms to 131s
- In-Circuit Serial Programming™ (ICSP™) via Two-Pins
- In-Circuit Debug via Two-Pins
- Operating Voltage Range: 2.0V to 3.6V
- 5.5V Tolerant Input (digital pins only)
- Selectable Open-Drain Configuration for Serial Communication and CCP Pins for Driving Outputs up to 5V
- On-Chip 2.5V Regulator

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Pin Diagrams – PIC18F6XJ90

64-Pin TQFP

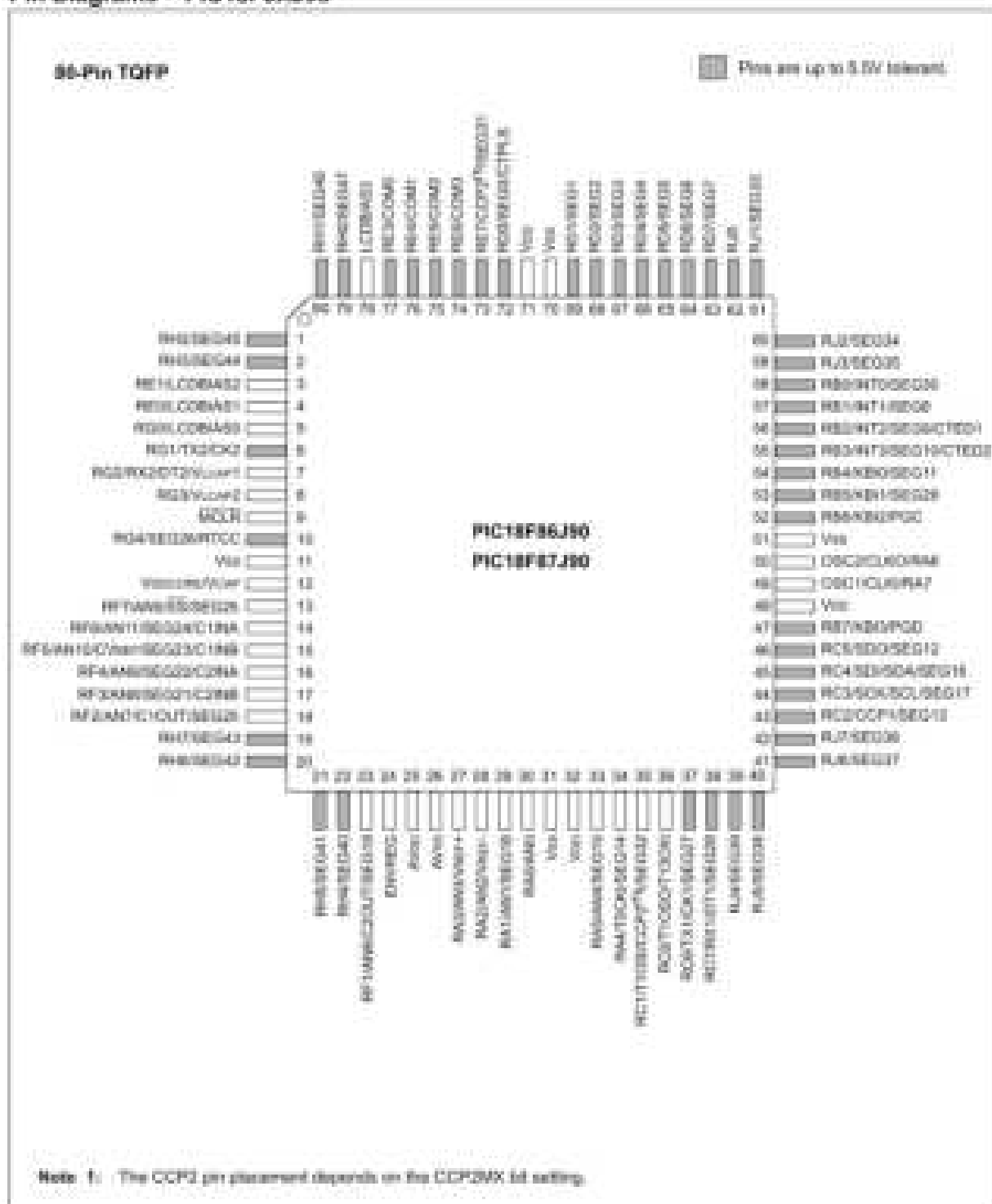
Pins are up to 5.5V tolerant.



Note 1: The CCP2 pin placement depends on the CCP2MS bit setting.

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Pin Diagrams – PIC18F8XJ90



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1.0 DEVICE OVERVIEW

This document contains device-specific information for the following devices:

- PIC18F86J90
- PIC18F86J90
- PIC18F87J90
- PIC18F87J90

This family combines the traditional advantages of all PIC18 microcontrollers – namely, high computational performance and a rich feature set – with a versatile, on-chip LCD driver, while maintaining an extremely competitive price point. These features make the PIC18F87J90 family a logical choice for many high-performance applications where price is a primary consideration.

1.1 Core Features

1.1.1 nanoWatt TECHNOLOGY

All of the devices in the PIC18F87J90 family incorporate a range of features that can significantly reduce power consumption during operation. Key items include:

- **Alternate Run Modes:** By clocking the controller from the Timer1 source or the internal RC oscillator, power consumption during code execution can be reduced by as much as 90%.
- **Multiple Idle Modes:** The controller can also run with its CPU core disabled but the peripherals still active. In these states, power consumption can be reduced even further, to as little as 4% of normal operation requirements.
- **On-the-Fly Mode Switching:** The power-managed modes are invoked by user code during operation, allowing the user to incorporate power-saving ideas into their application's software design.

1.1.2 OSCILLATOR OPTIONS AND FEATURES

All of the devices in the PIC18F87J90 family offer six different oscillator options, allowing users a range of choices in developing application hardware. These include:

- Two Crystal modes, using crystals or ceramic resonators.
- Two External Clock modes, offering the option of a divide-by-4 clock output.
- A Phase Lock Loop (PLL) frequency multiplier, available to the External Oscillator modes which allows clock speeds of up to 40 MHz. PLL can also be used with the internal oscillator.
- An internal oscillator block which provides an 8 MHz clock ($\pm 2\%$ accuracy) and an INTOSC source (approximately 31 kHz, stable over temperature and VDD), as well as a range of six user-selectable clock frequencies, between 125 kHz to 4 MHz, for a total of eight clock frequencies. This option frees the two oscillator pins for use as additional general purpose I/O.

The internal oscillator block provides a stable reference source that gives the family additional features for robust operation:

- **Fail-Safe Clock Monitor:** This option constantly monitors the main clock source against a reference signal provided by the internal oscillator. If a clock failure occurs, the controller is switched to the internal oscillator, allowing for continued low-speed operation or a safe application shutdown.
- **Two-Speed Start-up:** This option allows the internal oscillator to serve as the clock source from Power-on Reset, or wake-up from Sleep mode, until the primary clock source is available.

1.1.3 MEMORY OPTIONS

The PIC18F87J90 family provides ample room for application code, from 64 Kbytes to 128 Kbytes of code space. The Flash cells for program memory are rated to last up to 10,000 erase/write cycles. Data retention without refresh is conservatively estimated to be greater than 20 years.

The Flash program memory is readable and writable. During normal operation, the PIC18F87J90 family also provides plenty of room for dynamic application data with up to 3,823 bytes of data RAM.

1.1.4 EXTENDED INSTRUCTION SET

The PIC18F87J90 family implements the optional extension to the PIC18 instruction set, adding 8 new instructions and an Indexed Addressing mode. Enabled as a device configuration option, the extension has been specifically designed to optimize re-entrant application code originally developed in high-level languages, such as 'C'.

1.1.5 EASY MIGRATION

Regardless of the memory size, all devices share the same rich set of peripherals, allowing for a smooth migration path as applications grow and evolve.

The consistent pinout scheme used throughout the entire family also aids in migrating to the next larger device. This is true when moving between the 64-pin members, between the 60-pin members, or even jumping from 64-pin to 80-pin devices.

The PIC18F87J90 family is also largely pin-compatible with other PIC18 families, such as the PIC18F8720 and PIC18F8722, the PIC18F85J11, and the PIC18F8490 and PIC18F85J90 families of microcontrollers with LCD drivers. This allows a new dimension to the evolution of applications, allowing developers to select different price points within Microchip's PIC18 portfolio, while maintaining a similar feature set.

PIC18F87J90 FAMILY

1.2 LCD Driver

The on-chip LCD driver includes many features that make the integration of displays in low-power applications easier. These include an integrated voltage regulator with charge pump that allows contrast control in software and display operation above device V_{DD} .

1.3 Other Special Features

- **Communications:** The PIC18F87J90 family incorporates a range of serial communication peripherals, including an Addressable USART, a separate Enhanced USART that supports LIN/2602 specification 1.2, and one Master SSP module capable of both SPI and I²C™ (Master and Slave) modes of operation.
- **CCP Modules:** All devices in the family incorporate two Capture/Compare/PWM (CCP) modules. Up to four different time bases may be used to perform several different operations at once.
- **10-Bit A/D Converter:** This module incorporates programmable acquisition time, allowing for a channel to be selected and a conversion to be initiated without waiting for a sampling period and thus, reducing code overhead.
- **Charge Time Measurement Unit (CTMU):** The CTMU is a flexible analog module that provides accurate differential time measurement between pulse sources, as well as asynchronous pulse generation.
- **Extended Watchdog Timer (WDT):** This enhanced version incorporates a 16-bit prescaler, allowing an extended time-out range that is stable across operating voltage and temperature. See Section 28.6 “Electrical Characteristics” for time-out periods.
- **Real-Time Clock and Calendar Module (RTCC):** The RTCC module is intended for applications requiring that accurate time be maintained for extended periods of time with minimum to no intervention from the CPU.

The module is a 100-year clock and calendar with automatic leap year detection. The range of the clock is from 00:00:00 (midnight) on January 1, 2000 to 23:59:59 on December 31, 2099.

1.4 Details on Individual Family Members

Devices in the PIC18F87J90 family are available in 64-pin and 80-pin packages. Block diagrams for the two groups are shown in Figure 1-1 and Figure 1-2.

The devices are differentiated from each other in four ways:

1. Flash program memory (two sizes, 64 Kbytes for PIC18FX6J90 devices and 128 Kbytes for PIC18FX7J90 devices).
2. Data RAM (3,920 bytes RAM for both PIC18FX6J90 and PIC18FX7J90 devices).
3. I/O ports (7 bidirectional ports on PIC18FX6J90 devices, 9 bidirectional ports on PIC18FX7J90 devices).
4. LCD Pixels: 132 pixels (33 SEGs x 4 COMs) can be driven by 64-pin devices; 192 pixels (48 SEGs x 4 COMs) can be driven by 80-pin devices.

All other features for devices in this family are identical. These are summarized in Table 1-1 and Table 1-2.

The pinouts for all devices are listed in Table 1-3 and Table 1-4.

PIC18F87J90 FAMILY

TABLE 1-1: DEVICE FEATURES FOR THE PIC18F8XJ90 (64-PIN DEVICES)

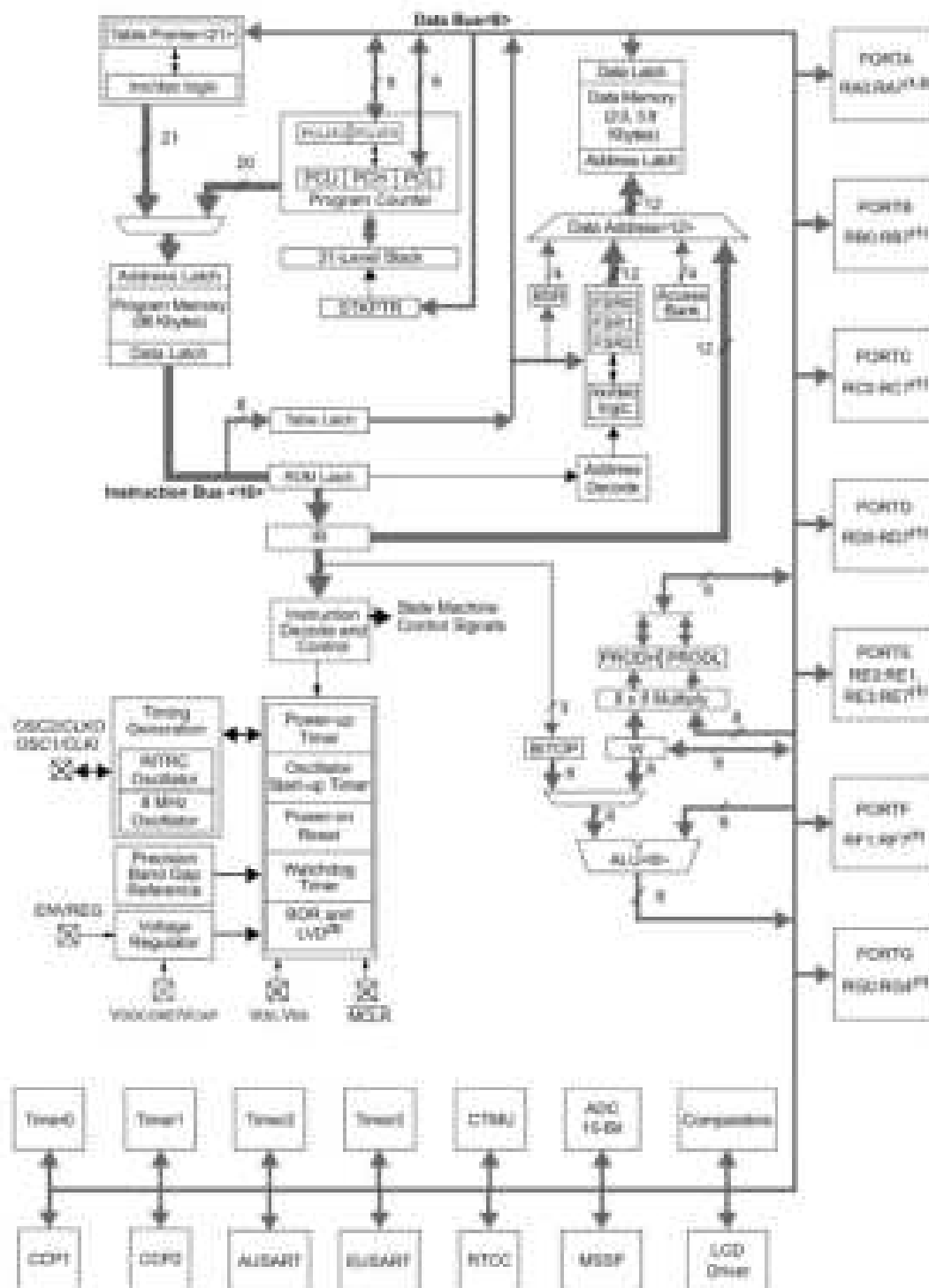
Features	PIC18F86J90	PIC18F87J90
Operating Frequency	DC – 48 MHz	
Program Memory (Bytes)	64K	128K
Program Memory (Instructions)	32,768	65,536
Data Memory (Bytes)	3,923	3,923
Interrupt Sources	29	
I/O Ports	Ports A, B, C, D, E, F, G	
LCD Driver (available pixels to drive)	132 (33 SEGs x 4 COMs)	
Timers	4	
Comparators	2	
CTMU	Yes	
RTCC	Yes	
Capture/Compare/PWM Modules	2	
Serial Communications	MSSP, Addressable USART, Enhanced USART	
10-Bit Analog-to-Digital Module	12 Input Channels	
Resets (and Delays)	POR, BOR, RESET Instruction, Stack Full, Stack Underflow, MCLR, WDT (PWRT, OST)	
Instruction Set	75 instructions, 83 with Extended Instruction Set Enabled	
Packages	64-Pin TQFP	

TABLE 1-2: DEVICE FEATURES FOR THE PIC18F8XJ90 (80-PIN DEVICES)

Features	PIC18F86J90	PIC18F87J90
Operating Frequency	DC – 48 MHz	
Program Memory (Bytes)	64K	128K
Program Memory (Instructions)	32,768	65,536
Data Memory (Bytes)	3,923	3,923
Interrupt Sources	29	
I/O Ports	Ports A, B, C, D, E, F, G, H, J	
LCD Driver (available pixels to drive)	182 (46 SEGs x 4 COMs)	
Timers	4	
Comparators	2	
CTMU	Yes	
RTCC	Yes	
Capture/Compare/PWM Modules	2	
Serial Communications	MSSP, Addressable USART, Enhanced USART	
10-Bit Analog-to-Digital Module	12 Input Channels	
Resets (and Delays)	POR, BOR, RESET Instruction, Stack Full, Stack Underflow, MCLR, WDT (PWRT, OST)	
Instruction Set	75 instructions, 83 with Extended Instruction Set Enabled	
Packages	80-Pin TQFP	

PIC18F87J90 FAMILY

FIGURE 1-1: PIC18F6XJ00 (64-PIN) BLOCK DIAGRAM



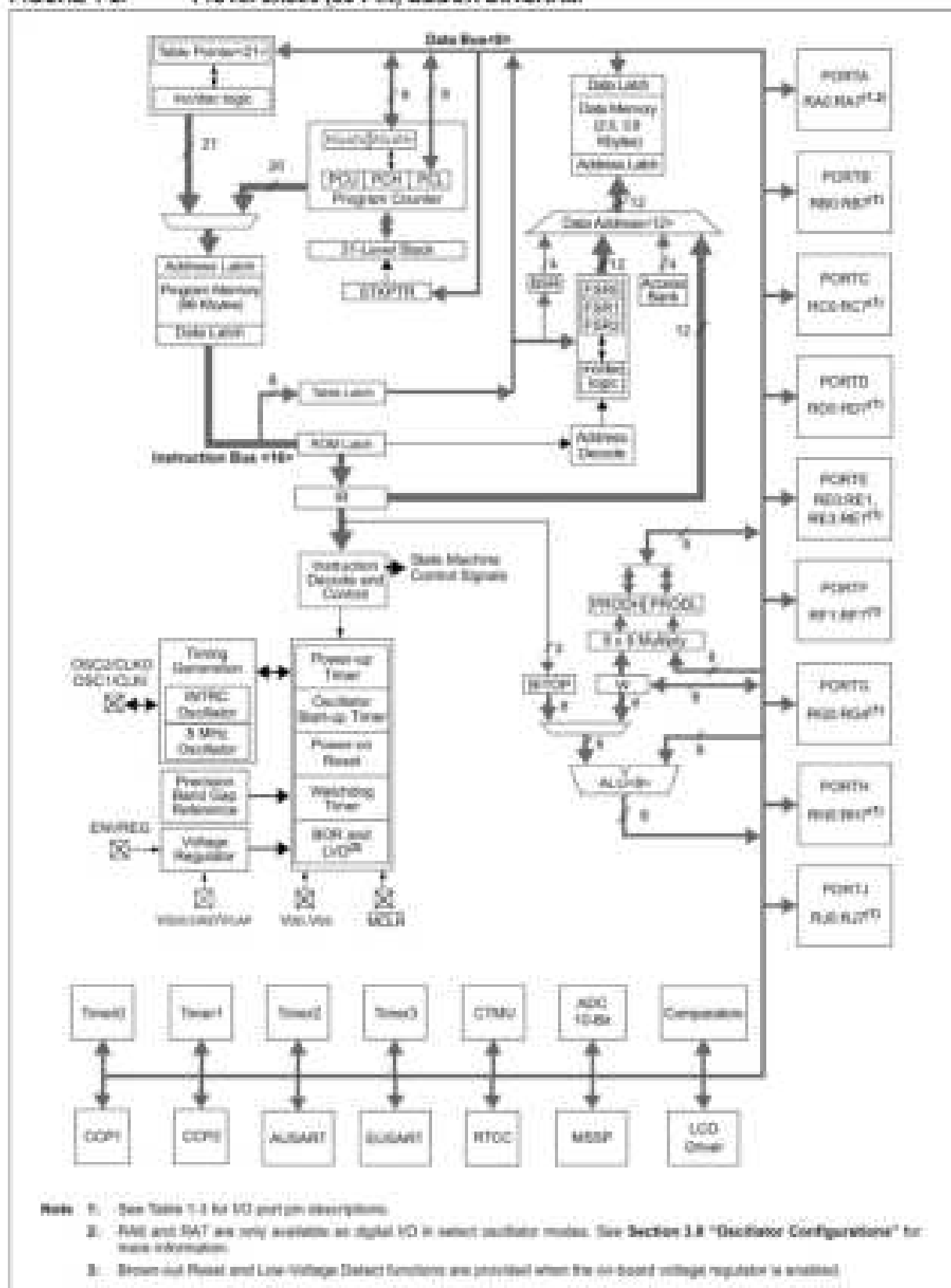
Model 1: Same Types 1-3 for all part-ers independently

2) R4A and R4B are only available as digital I/O to select multiple modes. See Section 3.0 "Oscillator Configurations" for more information.

1. **Universal Reset and Low-Voltage Output Functions** are provided when the dedicated voltage regulator is enabled.

PIC18F87J90 FAMILY

FIGURE 1-2: PIC18F8XJ00 (80-PIN) BLOCK DIAGRAM



PIC18F87J90 FAMILY

TABLE 1-3: PIC18F6XJ90 PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number TQFP	Pin Type	Buffer Type	Description
MCLR	7	I	ST	Master Clear (input) or programming voltage (input). This pin is an active-low Reset to the device.
OSC1/CLKIN/RA7 OSC1 CLKI	39	I I	CMOS CMOS	Oscillator crystal or external clock input. Oscillator crystal input. External clock source input. Always associated with pin function, OSC1. (See related OSC1/CLKI, OSC2/CLKO pins.)
RA7		IO	TTL	General purpose I/O pin.
OSC2/CLKO/RA6 OSC2 CLKO	40	O O	— —	Oscillator crystal or clock output. Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. In EC modes, OSC2 pin outputs CLKI, which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate.
RA6		IO	TTL	General purpose I/O pin.
RA0/AN0 RA0 AN0	24	IO I	TTL Analog	PORTA is a bidirectional I/O port. Digital I/O. Analog Input 0.
RA1/AN1/SEG18 RA1 AN1 SEG18	23	IO I O	TTL Analog Analog	Digital I/O. Analog Input 1. SEG18 output for LCD.
RA2/AN2/VREF- RA2 AN2 VREF-	22	IO I I	TTL Analog Analog	Digital I/O. Analog Input 2. A/D reference voltage (low) input.
RA3/AN3/VREF+ RA3 AN3 VREF+	21	IO I I	TTL Analog Analog	Digital I/O. Analog Input 3. A/D reference voltage (high) input.
RA4/T0CKI/SEG14 RA4 T0CKI SEG14	28	IO I O	ST ST Analog	Digital I/O. Timer0 external clock input. SEG14 output for LCD.
RA5/AN4/SEG15 RA5 AN4 SEG15	27	IO I O	TTL Analog Analog	Digital I/O. Analog Input 4. SEG15 output for LCD.
RA6				See the OSC2/CLKO/RA6 pin.
RA7				See the OSC1/CLKI/RA7 pin.

Legend: TTL = TTL compatible input
ST = Schmitt Trigger input with CMOS levels
I = Input
P = Power
PC™ = I²C/SMBus
CMOS = CMOS compatible input or output
Analog = Analog input
O = Output
OD = Open-Drain (no P diode to VDD)

Note 1: Default assignment for CCP2 when the CCP2MX Configuration bit is set.

2: Alternate assignment for CCP2 when the CCP2MX Configuration bit is cleared.