PRODUCT SPECIFICATION

TFT LCD MODULE

MODEL : KWH032ST05-F02 Version: 2.0

【 ◆ 】 Preliminary Specification

【 】 Finally Specification

CUSTOMER'S APPROVAL	
SIGNATURE:	DATE:

●It signifies that you fully understand and accept all the contents of this specification if you sign and send back the first page of this specifications.

Designed by	R&D Checked by	Quality Department by	Approved by
LEO			

Prepared By :

FORMIKE ELECTRONIC CO.,LTD

Address : Flat 401-403, 4th Floor, Block B, iPARK Building, DengLiang Rd.,No.26, NanShan District, ShenZhen, 518054,China

TEL:(86) 755 88306921,88306931 FAX:(86) 755 88304615

Http:// www.wandisplay.com

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Revision record

REV NO.	REV DATE	CONTENTS	Note
A	**2012-06-18**	**NEW ISSUE**	
B	**2015-06-18**	**Modify the POL,INSPECTION**	**LEO**

Table Of Contents

1. General Description

1.1 Description

KWH032ST05-F01 is a Transmissive type color active matrix liquid crystal display (LCD), which uses amorphous thin film transistor (TFT) as switching devices. This product is composed of a TFT LCD panel, driver IC, FPC and backlight unit .
The following table described the features of FORMIKE KWH032ST05-F01.

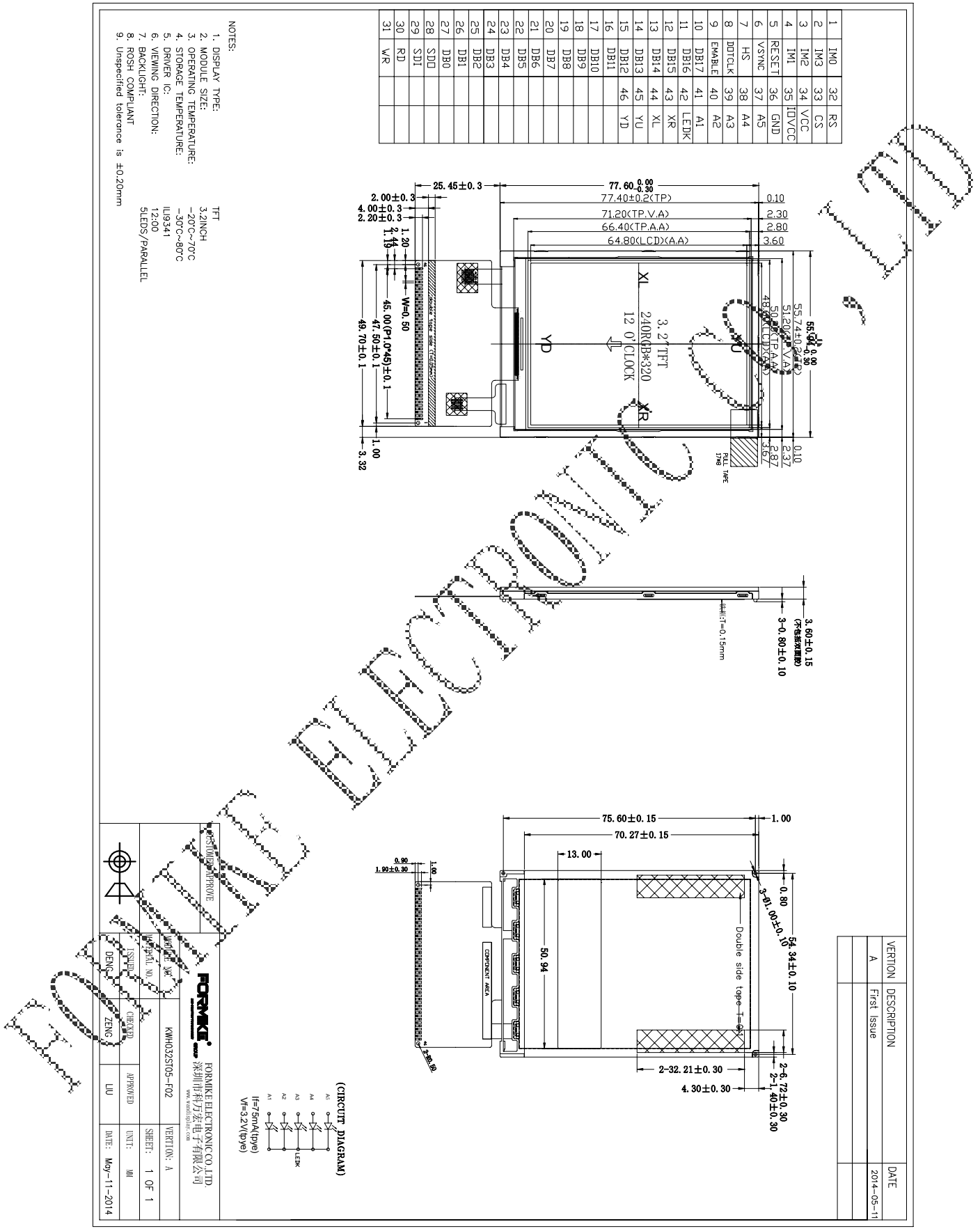
1.2 Application

Mobile phone, Multimedia products
and other electronic Products
Etc.

1.3 Features:

Features	Description	UNITS
LCD type	3.2"TFT	--
Dot arrangement	240（RGB）×320	dots
Driver IC	ILI9341	--
Color Depth	65K/262K	
Interface	RGB, Serial and MCU Interface	
View Direction	12 O'clock	
Module size	55.94(W) ×77.60 (H)×3.6(T)	mm
Active area	48.60(W) ×64.80 (H)	mm
Dot pitch	0.2025 (W) ×0.2025 (H)	mm
Back Light	5 White LED In parallel	--
With/Without TSP	With TSP	
Weight(g)	TBD	

2. External Dimensions



1	IM0	32	RS
2	IM3	33	CS
3	IM2	34	VCC
4	IM1	35	IOVCC
5	RESET	36	GND
6	VSYNC	37	A5
7	HS	38	A4
8	DOTCLK	39	A3
9	EMABLE	40	A2
10	DB17	41	A1
11	DB16	42	LEDK
12	DB15	43	XR
13	DB14	44	XL
14	DB13	45	YU
15	DB12	46	YD
16	DB11		
17	DB10		
18	DB9		
19	DB8		
20	DB7		
21	DB6		
22	DB5		
23	DB4		
24	DB3		
25	DB2		
26	DB1		
27	DB0		
28	SDO		
29	SDI		
30	RD		
31	WR		

3. Interface Description

PIN NO.	PIN NAME	DESCRIPTION
1	IM0	The selection of the given interfaces are done by external IM[3:0] Pins and shown as below Note 1.
2	IM3	
3	IM2	
4	IM1	
5	RESET	This signal will reset the device and must be applied to properly initialize the chip. Signal is active low.
6	VSYNC	Frame synchronizing signal for RGB interface operation. Fix to IOVCC or GND level when not in use.
7	HSYNC	Line synchronizing signal for RGB interface operation. Fix to IOVCC or GND level when not in use.
8	DOTCLK	Dot clock signal for RGB interface operation. Fix to IOVCC or GND level when not in use.
9	ENABLE	Data enable signal for RGB interface operation. Fix to IOVCC or GND level when not in use.
10-27	DB17-DB0	18-Bit parallel data bus for MCU system and RGB interface mode. Fix to GND level when not in use.
28	SDO	Serial output signal. The data is outputted on the falling edge of the SCL signal. If not used, open this pin.
29	SDI	The data is applied on the rising edge of the SCL signal. Fix to IOVCC or GND level when not in use.
30	RD	8080-I/8080-II system(RD):Serves as a read signal and MCU read data at the rising edge. Fix to IOVCC level when not in use.
31	WR	8080-I/8080-II system(WR):Serves as a write signal and writes data at the rising edge. 4-Line system(RS):Serves as command or parameter select. Fix to IOVCC level when not in use.
32	RS	This pin is used to select ”data or command” in the parallel interface or 4-wire 8-bit serial data interface. When RS=”1”, data is selected. When RS=”0”, command is selected. This pin is used serial interface clock in 3-wire 9-bit/4-wire 8-bit serial data interface. Fix to IOVCC or GND level when not in use.
33	CS	Chip select input pin(“ low” enable).
34	VCC	Power supply Voltage for I/O Interface (+1.65V~+2.8V).
35	IOVCC	System Power supply Voltage (+2.5V~+3.3V).
36	GND	System ground.
37	A5	Power supply for LED backlight Anode input.
38	A4	Power supply for LED backlight Anode input.
39	A3	Power supply for LED backlight Anode input.
40	A2	Power supply for LED backlight Anode input.

41	A1	Power supply for LED backlight Anode input.
42	K	Power supply for LED backlight Cathode input.
43	XR	Touch Panel Right Side Wire.
44	XL	Touch Panel Left Side Wire.
45	YU	Touch Panel Up Side Wire.
46	YD	Touch Panel Down Side Wire.

Note 1:

ILI9341 provides four kinds of MCU system interface with 8080- Ⅰ /8080- Ⅱ series parallel interface and 3-/4-line serial interface. The selection of the given interfaces are done by external IM [3:0] pins and shown as below:

IM3	IM2	IM1	IM0	MCU-Interface Mode	Pins in use	
					Register/Content	GRAM
0	0	0	0	8080 MCU 8-bit bus Interface Ⅰ	D[7:0]	D[7:0],WRX,RDX,CSX,D/CX
0	0	0	1	8080 MCU 16-bit bus Interface Ⅰ	D[7:0]	D[15:0],WRX,RDX,CSX,D/CX
0	0	1	0	8080 MCU 9-bit bus Interface Ⅰ	D[7:0]	D[8:0],WRX,RDX,CSX,D/CX
0	0	1	1	8080 MCU 18-bit bus Interface Ⅰ	D[7:0]	D[17:0],WRX,RDX,CSX,D/CX
0	1	0	1	3-wire 9-bit data serial interface Ⅰ	SCL,SDA,CSX	
0	1	1	0	4-wire 8-bit data serial interface Ⅰ	SCL,SDA,D/CX,CSX	
1	0	0	0	8080 MCU 16-bit bus Interface Ⅱ	D[8:1]	D[17:10],D[8:1],WRX,RDX,CSX,D/CX
1	0	0	1	8080 MCU 8-bit bus Interface Ⅱ	D[17:10]	D[17:10],WRX,RDX,CSX,D/CX
1	0	1	0	8080 MCU 18-bit bus Interface Ⅱ	D[8:1]	D[17:0],WRX,RDX,CSX,D/CX
1	0	1	1	8080 MCU 9-bit bus Interface Ⅱ	D[17:10]	D[17:9],WRX,RDX,CSX,D/CX
1	1	0	1	3-wire 9-bit data serial interface Ⅱ	SCL,SDI,SDO, CSX	
1	1	1	0	4-wire 8-bit data serial interface Ⅱ	SCL,SDI,D/CX,SDO, CSX	

4. Absolute Maximum Ratings

The absolute maximum rating is listed on following table. When ILI9341 is used out of the absolute maximum ratings, ILI9341 may be permanently damaged. To use ILI9341 within the following electrical characteristics limitation is strongly recommended for normal operation. If these electrical characteristic conditions are exceeded during normal operation, ILI9341 will malfunction and cause poor reliability.

Item	Symbol	Unit	Value
Supply voltage	VCI	V	-0.3 ~ +4.6
Supply voltage (Logic)	VDDI	V	-0.3 ~ +4.6
Supply voltage (Digital)	VCORE	V	-0.3 ~ +2.0
Driver supply voltage	VGH-VGL	V	-0.3 ~ +32.0
Logic input voltage range	VIN	V	-0.3 ~ VDDI + 0.3
Logic output voltage range	VO	V	-0.3 ~ VDDI + 0.3
Operating temperature	Topr	°C	-40 ~ +85
Storage temperature	Tstg	°C	-55 ~ +110

Note: If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

5. Electrical Characteristics

Item	Symbol	Unit	Condition	Min.	Typ.	Max.	Note
Power and Operation Voltage							
Analog Operating Voltage	VCI	V	Operating voltage	2.5	2.8	3.3	Note2
Logic Operating Voltage	VDDI	V	I/O supply voltage	1.65	2.8	3.3	Note2
Digital Operating voltage	VCORE	V	Digital supply voltage	-	1.5	-	Note2
Gate Driver High Voltage	VGH	V	-	10.0	-	16.0	Note3
Gate Driver Low Voltage	VGL	V	-	-10.0	-	-5.0	Note3
Driver Supply Voltage	-	V	VGH-VGL	15	-	28	Note3
Current consumption during standby mode	Ist	μA	VCI=2.8V , Ta=25°C	-	-	100	-
Input and Output							
Logic High Level Input Voltage	VIH	V	-	0.7*VDDI	-	VDDI	Note1,2,3
Logic Low Level Input Voltage	VIL	V	-	VSS	-	0.3*VDDI	Note1,2,3
Logic High Level Output Voltage	VOH	V	IOL=-1.0mA	0.8*VDDI	-	VDDI	Note1,2,3
Logic Low Level Output Voltage	VOL	V	IOL=1.0mA	VSS	-	0.2*VDDI	Note1,2,3
Logic High Level Input Current	IIH	μA	-	-	-	1	Note1,2,3
Logic Low Level Input Current	IIL	μA	-	-1	-	-	Note1,2,3
Logic Input Leakage Current	ILEA	μA	VIN=VDDI or VSS	-0.1	-	+0.1	Note1,2,3
VCOM Operation							
VCOM High Voltage	VCOMH	V	Ccom=12nF	2.5	-	5.0	Note8
VCOM Low Voltage	VCOML	V	Ccom=12nF	-2.5	-	0.0	Note8
VCOM Amplitude Voltage	VCOMA	V	|VCOMH-VCOML|	4.0	-	5.5	Note3
Source Driver							
Source Output Range	Vsout	V	-	0.1	-	DDVDH-0.1	Note1
Gamma Reference Voltage	GVDD	V	-	3.0	-	5.0	Note3
Output Deviation Voltage (Source Output channel)	Vdev	mV	Sout=4.2V Sout=0.8V 4.2V>Sout>0.8V	-	-	20 15	Note4 -
Output Offset Voltage	VOFSET	mV	-	-	-	35	Note7
Booster Operation							
1st Booster (VCI x2) Voltage	DDVDH	V	-	4.95 (Note 5)	-	5.8 (Note 6)	Note8
1st Booster (VCI x2 Drop Voltage	VCI x2 drop	%	loading=1mA	-	-	5	Note8
Liner Range	Vliner	V	-	0.2	-	DDVDH-0.2	

Note 1: VDDI=1.65 to 3.3V, VCI=2.5 to 3.3V, AGND=VSS=0V, Ta= -30 to 70 (to -85 no damage) °C.

Note2: Please supply digital VDDI voltage equal or less than analog VCI voltage.

Note3: CSX, RDX, WRX, D[17:0], DCX, RESX, TE, DOTCLK, VSYNC, HSYNC, DE, SDA, SCL (M3, M2, M1, M0), and Test pins.

Note4: When the measurements are performed with LCD module, Measurement Points are like Note3.

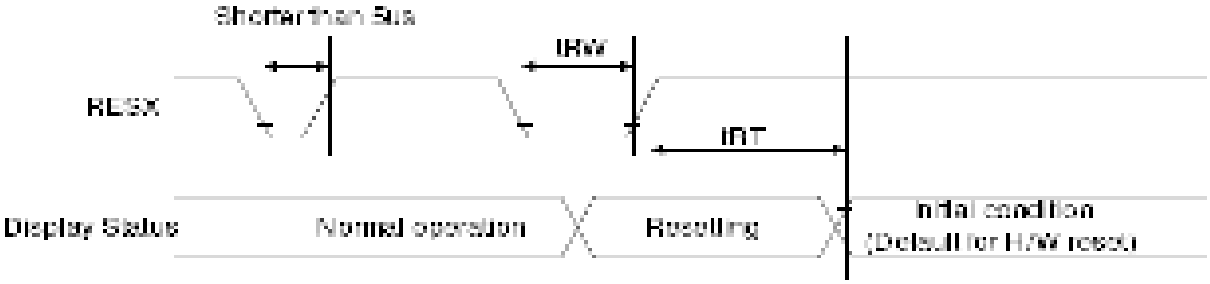
Note5: VCI=2.6V

Note6: VCI=3.3V

Note7: The Max. Value is between with Note 4 measure point and Gamma setting value

6.Timing Characteristics.

6.1 Reset Timing Characteristics.



Signal	Symbol	Parameter	Min	Max	Unit
RESX	tRW	Reset pulse duration	10		uS
	tRT	Reset cancel		5 (note 1,5)	mS
				120 (note 1,6,7)	mS

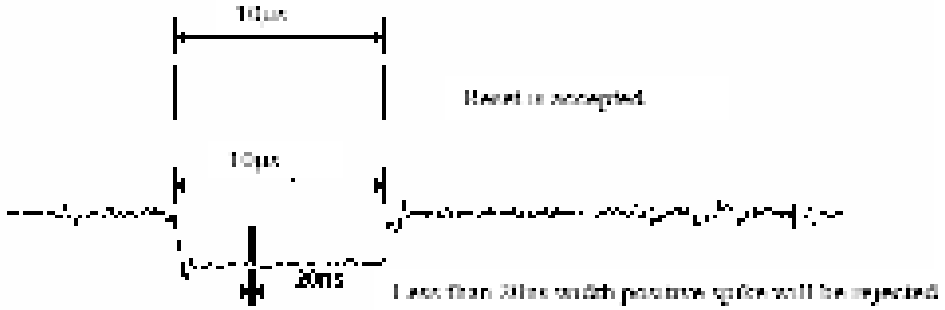
Note 1: The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NV memory to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.

Note 2: Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 10us	Reset
Between 5us and 10us	Reset starts

Note 3: During the "Resetting" period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out -mode. The display remains the blank state in Sleep In -mode.) And then return to Default condition for Hardware Reset.

Note 4: Spike Rejection also applies during a valid reset pulse as shown below:



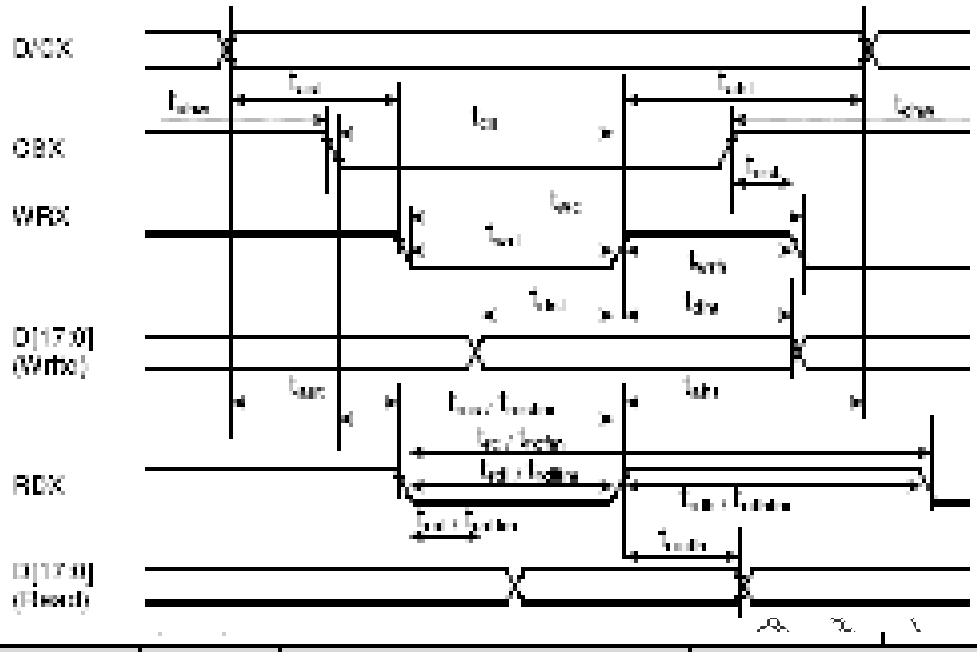
Note 5: When Reset applied during Sleep In Mode.

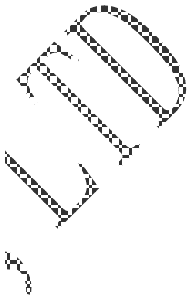
Note 6: When Reset applied during Sleep Out Mode.

Note 7: It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

6.2. i80-System Interface Timing Characteristics.

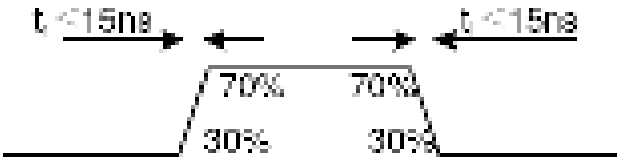
Display Parallel 18/16/9/8-bit Interface Timing Characteristics (8080- T system)



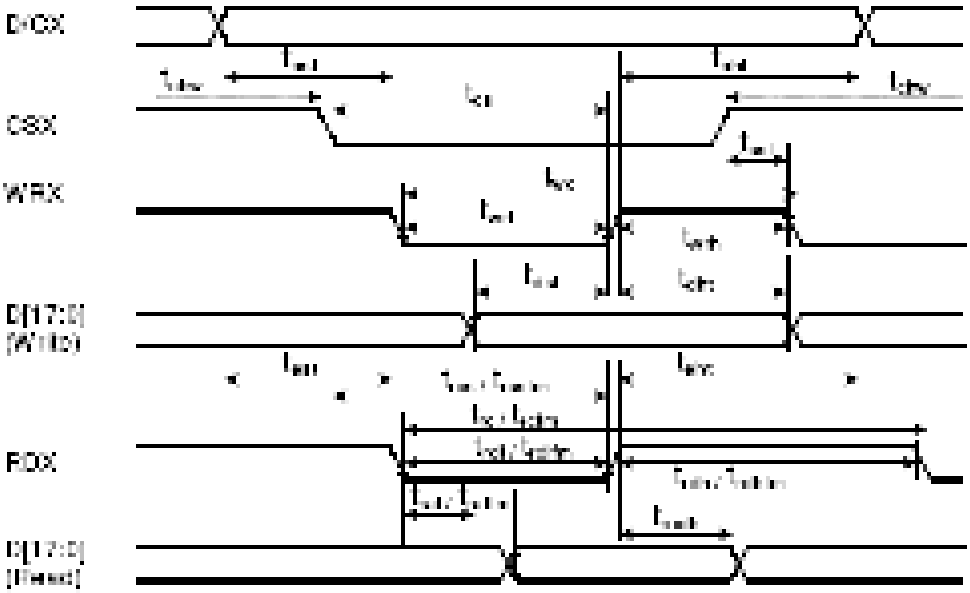


Signal	Symbol	Parameter	min	max	Unit	Description
DCX	tdst	Address setup time	0	-	ns	
	tdht	Address hold time (Write/Read)	0	-	ns	
CSX	tchw	CSX "H" pulse width	0	-	ns	
	tcs	Chip Select setup time (Write)	15	-	ns	
	trcs	Chip Select setup time (Read ID)	45	-	ns	
	trcsfm	Chip Select setup time (Read FM)	355	-	ns	
	tcsf	Chip Select Wait time (Write/Read)	10	-	ns	
WRX	twc	Write cycle	66	-	ns	
	twrh	Write Control pulse H duration	15	-	ns	
	twrl	Write Control pulse L duration	15	-	ns	
RDX (FM)	trcfm	Read Cycle (FM)	450	-	ns	
	trdhfm	Read Control H duration (FM)	90	-	ns	
	trdlfm	Read Control L duration (FM)	355	-	ns	
RDX (ID)	trc	Read cycle (ID)	160	-	ns	
	rdh	Read Control pulse H duration	90	-	ns	
	rdl	Read Control pulse L duration	45	-	ns	
D[17:3], D[16:3], D[8:0], D[7:0]	tdst	Write data setup time	10	-	ns	For maximum CL=30pF For minimum CL=8pF
	tdht	Write data hold time	10	-	ns	
	trac	Read access time	-	40	ns	
	tracfm	Read access time	-	340	ns	
	tod	Read output disable time	20	80	ns	

Note: Ta = -30 to 70 °C, VDDI= 1.65V to 3.3V, VCI=2.5V to 3.3V, VSS=0V

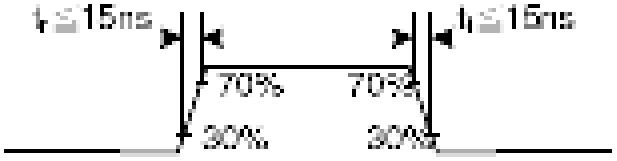


Display Parallel 18/16/9/8-bit Interface Timing Characteristics(8080-II system)



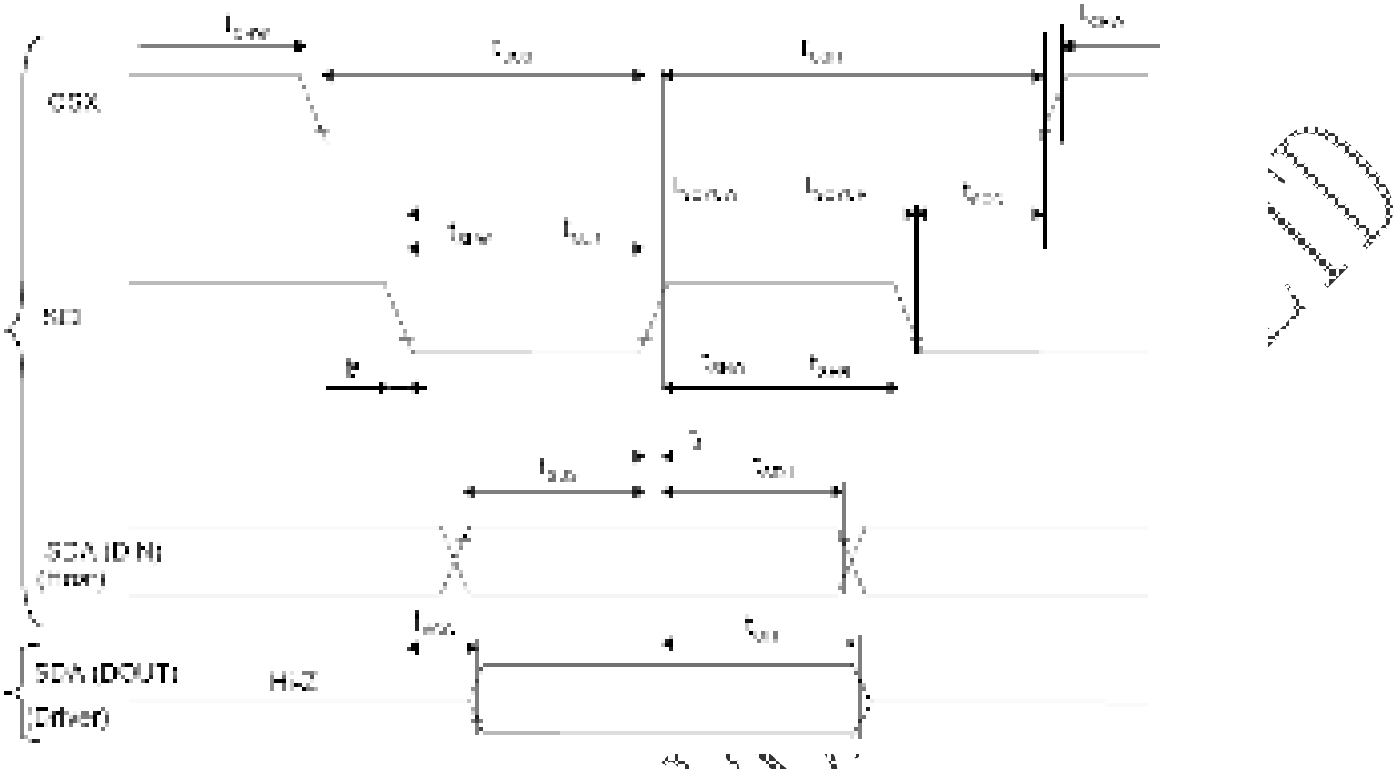
Signal	Symbol	Parameter	min	max	Unit	Description
D/CX	tast	Address setup time	0	-	ns	
	tsht	Address hold time (Write/Read)	0	-	ns	
CSX	tcsw	CSX "H" pulse width	0	-	ns	
	tcs	Chip Select setup time (Write)	15	-	ns	
	trcs	Chip Select setup time (Read ID)	45	-	ns	
	trcsfm	Chip Select setup time (Read FM)	355	-	ns	
	tcsf	Chip Select Wait time (Write/Read)	10	-	ns	
WRX	twc	Write cycle	66	-	ns	
	twrh	Write Control pulse H duration	15	-	ns	
	twrl	Write Control pulse L duration	15	-	ns	
RDX (FM)	trdfm	Read Cycle (FM)	450	-	ns	
	trdhfm	Read Control H duration (FM)	90	-	ns	
	trdlfm	Read Control L duration (FM)	355	-	ns	
RDX (ID)	trd	Read cycle (ID)	160	-	ns	
	trdh	Read Control pulse H duration	90	-	ns	
	trdl	Read Control pulse L duration	45	-	ns	
D[17:0] D[17:10][8:0][8:1], D[17:10], D[17:9]	tdsw	Write data setup time	10	-	ns	For maximum CL=30pF For minimum CL=8pF
	tdhw	Write data hold time	10	-	ns	
	trd	Read access time	-	40	ns	
	trdfm	Read access time	-	340	ns	
	trod	Read output disable time	20	80	ns	

Note: Ta = -30 to 70 °C, VDD=1.65V to 3.3V, VCI=2.5V to 3.3V, VSS=0V.



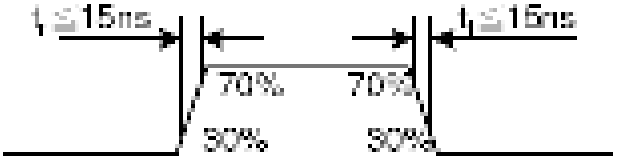
6.3. SPI Interface Timing Characteristics.

Display Serial Interface Timing Characteristics (3-line SPI system)

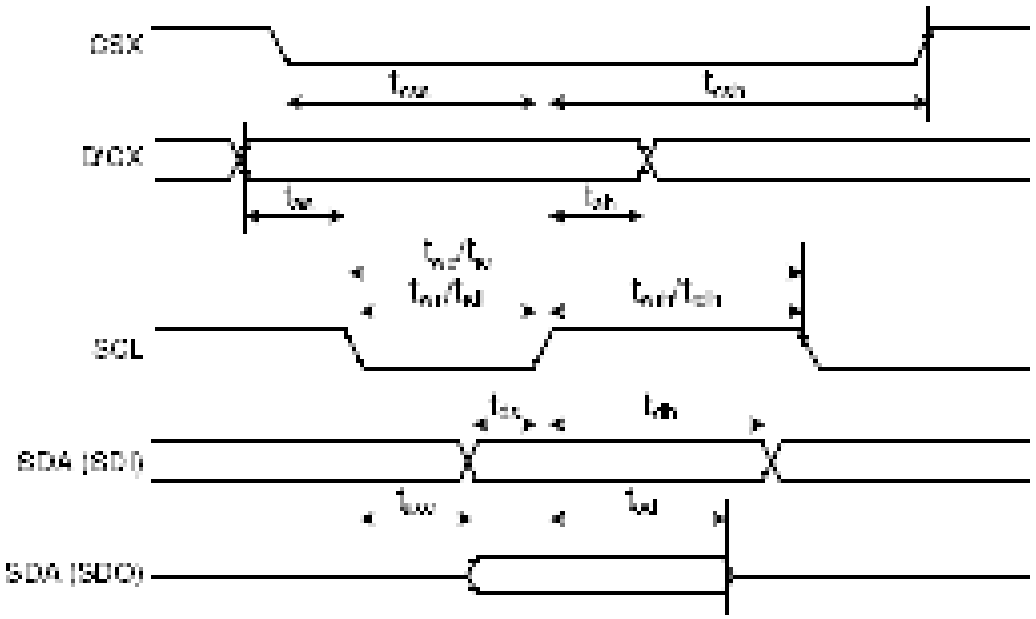


Signal	Symbol	Parameter	min	max	Unit	Description
SCL	tscycw	Serial Clock Cycle (Write)	100	-	ns	
	tshw	SCL "H" Pulse Width (Write)	40	-	ns	
	tslw	SCL "L" Pulse Width (Write)	40	-	ns	
	tscycr	Serial Clock Cycle (Read)	150	-	ns	
	tshr	SCL "H" Pulse Width (Read)	60	-	ns	
	tslr	SCL "L" Pulse Width (Read)	60	-	ns	
SDA (SDI) (Input)	tsds	Data setup time (Write)	30	-	ns	
	tsdh	Data hold time (Write)	30	-	ns	
SDA (SDO) (Output)	tacc	Access time (Read)	10	-	ns	
	tdh	Output disable time (Read)	10	50	ns	
CSX	tcsr	SCL-CSX	20	-	ns	
	tchw	CSX "H" Pulse Width	40	-	ns	
	tcss	CSX-SCL Time	60	-	ns	
	tsch		60	-	ns	

Note: Ta = 25°C, VDDI=1.65V to 3.3V, VCI=2.6V to 3.3V, AGND=VSS=0V

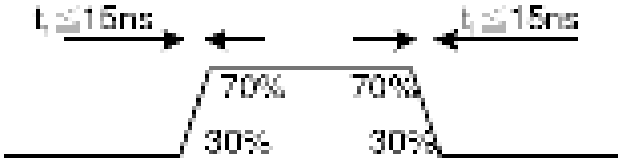


Display Serial Interface Timing Characteristics (4-line SPI system)

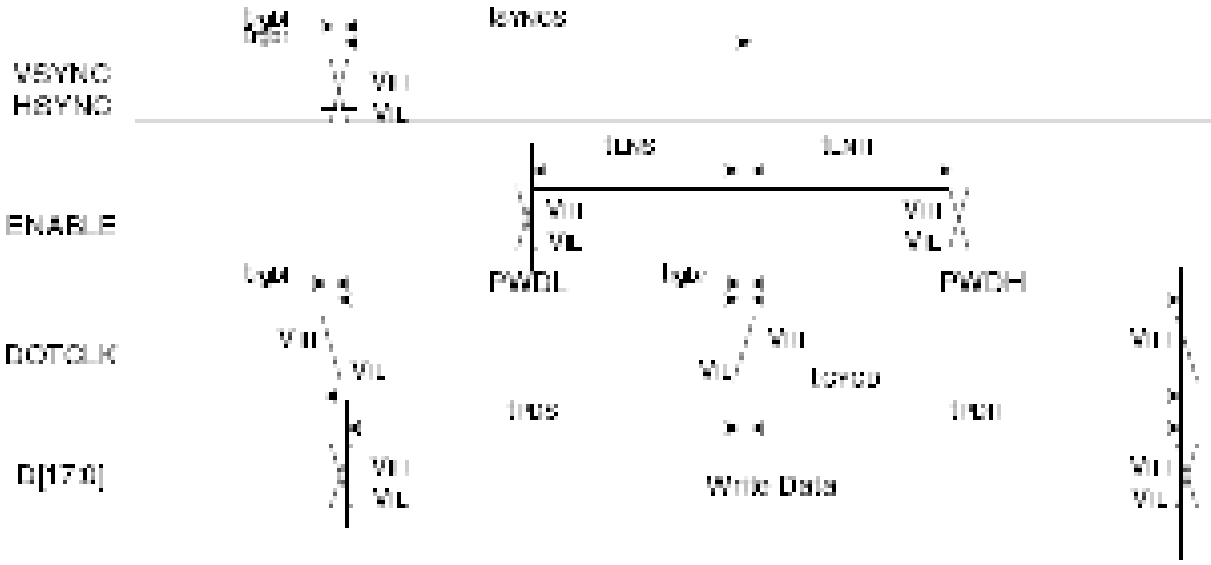


Signal	Symbol	Parameter	min	max	Unit	Description
CSX	tcss	Chip select time (Write)	60	-	ns	
	tcsh	Chip select hold time (Read)	40	-	ns	
SCL	tscc	Serial clock cycle (Write)	100	-	ns	
	tshw	SCL "H" pulse width (Write)	40	-	ns	
	tslw	SCL "L" pulse width (Write)	40	-	ns	
	tscr	Serial clock cycle (Read)	150	-	ns	
	tshr	SCL "H" pulse width (Read)	60	-	ns	
	tsrd	SCL "L" pulse width (Read)	60	-	ns	
DCX	tscs	DCX setup time	10	-		
	tsch	DCX hold time (Write / Read)	10	-		
SDA (SDI) (Input)	tdss	Data setup time (Write)	30	-	ns	
	tdsh	Data hold time (Write)	80	-	ns	
SDA (SDO) (Output)	tacc	Access time (Read)	10	-	ns	For maximum CL=30pF
	tod	Output disable time (Read)	10	50	ns	For minimum CL=8pF

Note: Ta = 25 °C, VDDI= 1.65V to 3.3V, VCI=2.5V to 3.3V, AGND=VSS=0V

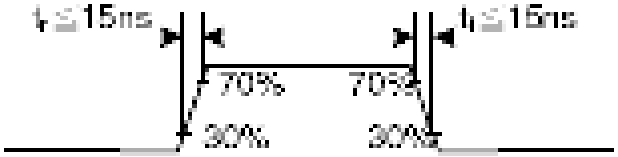


6.4. RGB Interface Timing Characteristics.



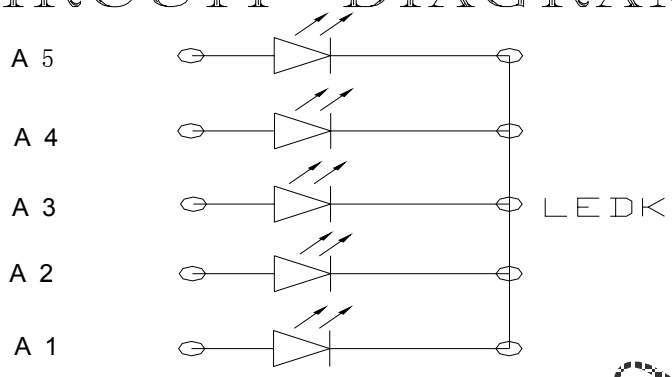
Signal	Symbol	Parameter	min	max	Unit	Description
VSYNC / HSYNC		VSYNC/HSYNC setup time	15	-	ns	16/18/24-bit bus RGB interface mode
		VSYNC/HSYNC hold time	15	-	ns	
DE		DE setup time	15	-	ns	
		DE hold time	15	-	ns	
D[17:0]		Data setup time	15	-	ns	
		Data hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level period	15	-	ns	
	PWDL	DOTCLK low-level period	15	-	ns	
		DOTCLK cycle time	100	-	ns	
		DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns	
VSYNC / HSYNC		VSYNC/HSYNC setup time	15	-	ns	6-bit bus RGB interface mode
		VSYNC/HSYNC hold time	15	-	ns	
DE		DE setup time	15	-	ns	
		DE hold time	15	-	ns	
D[17:0]		Data setup time	15	-	ns	
		Data hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level pulse period	15	-	ns	
	PWDL	DOTCLK low-level pulse period	15	-	ns	
		DOTCLK cycle time	100	-	ns	
		DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns	

Note: Ta = -30 to 70°C, VDDI=1.65V to 3.3V, VCI=2.5V to 3.3V, AGND=VSS=0V



7. Backlight Characteristics.

(CIRCUIT DIAGRAM)



If=75mA(tpye)
Vf=3.2V(tpye)

Item	Symbol	MIN	TYP	MAX	UNIT	Test Condition	Note
Supply Voltage	**Vf**	**3.0**	**3.2**	**3.4**	**V**	**If=75 mA**	**-**
Supply Current	**If**	**-**	**75**	**-**	**mA**	**-**	**-**
Reverse Voltage	**Vr**	**-**	**-**	**5**	**V**	**10uA**	
Power dissipation	**Pd**	**-**	**240**	**-**	**mW**	**-**	
Luminous Intensity for LCM		**230**	**260**	**390**	**Cd/m²**	**If=75 mA**	
Uniformity for LCM	**-**	**80**	**-**	**-**	**%**	**If=75 mA**	
Life Time	**-**	**20000**	**-**	**-**	**Hr**	**If=75 mA**	**-**
Backlight Color	**X**	**0.27**	**0.29**	**0.31**	**-**	**If=75 mA**	
	Y	**0.27**	**0.29**	**0.31**	**-**	**If=75 mA**	

8.Optical Characteristics

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Transmittance (without Polarizer)		T(%)	—	—	18.0	—	—	
Contrast Ratio		CR	Θ=0	400	500	—	—	(1)(2)
Response time	Rising	T_R	Normal viewing angle	—	4	8	msec	(1)(3)
	Falling	T_F	—	—	12	24		
Color gamut		S(%)			60		%	
Color chromaticity (CIE1931)	White	W_x		0.283	0.303	0.323		(1)(4) CF glass (C-light)
		Wy		0.305	0.325	0.345		
	Red	Rx		0.606	0.626	0.646		
		Ry		0.314	0.334	0.354		
	Green	Gx		0.257	0.277	0.297		
		Gy		0.529	0.549	0.569		
	Blue	Bx		0.122	0.142	0.162		
		By		0.102	0.122	0.142		
Viewing angle	Hor.	Θ_L	CR>10	35	70	—		
		Θ_R		35	70	—		
	Ver.	Θ_U		35	70	—		
		Θ_D		10	55	—		
Optima View Direction		12 O'clock						(5)

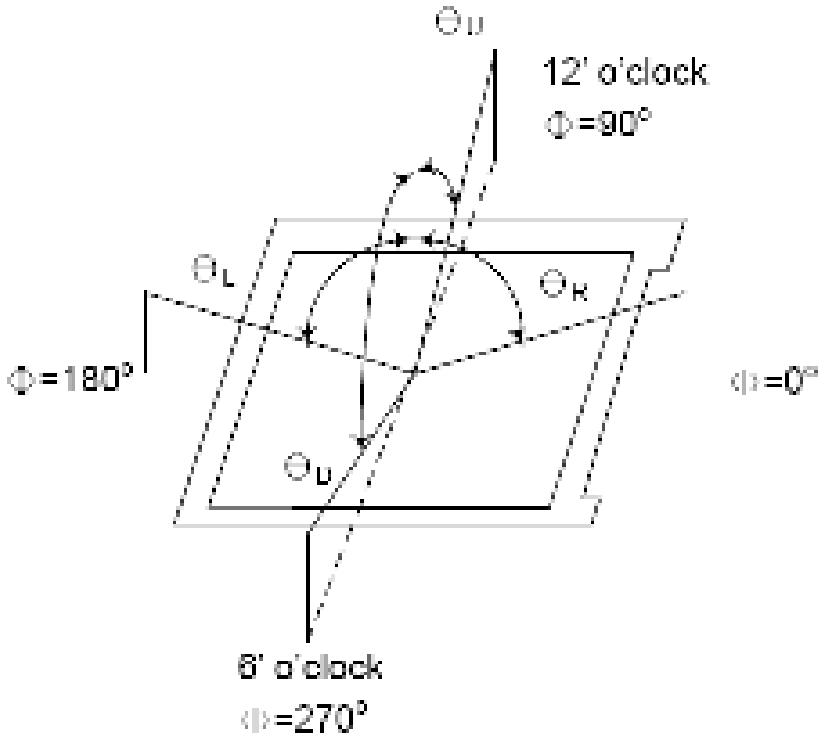
4.2 Measuring Condition

- Measuring surrounding : dark room
- Ambient temperature : 25±2°C
- 15min. warm-up time.

4.3 Measuring Equipment

- FPM520 of Westar Display technologies. INC., which utilized SR-3 for Chromaticity and BM-5A for other optical characteristics.

Note (1) Definition of Viewing Angle :

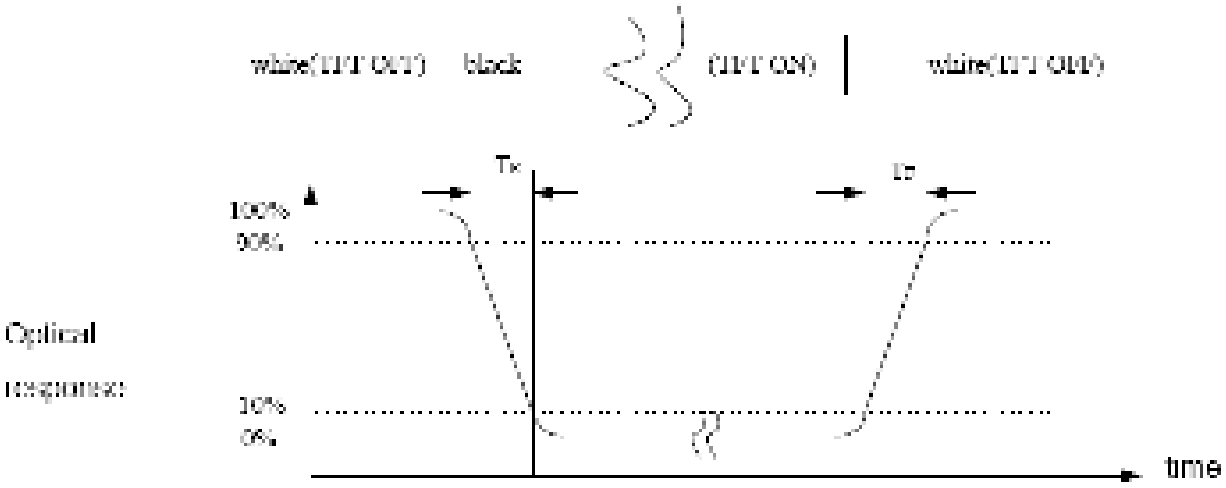


Note (2) Definition of Contrast Ratio(CR) :

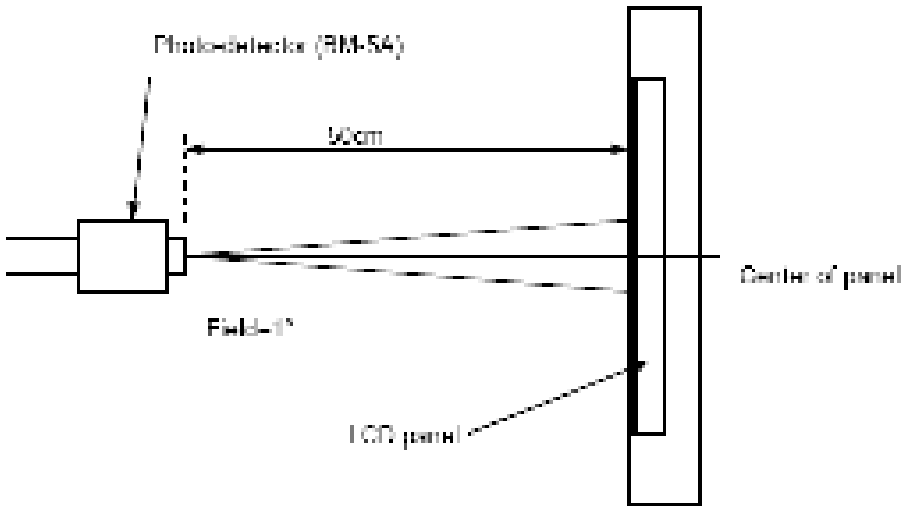
measured at the center point of panel

$$CR = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

Note (3) Definition of Response Time : Sum of T_{ll} and T_l



Note (4) Definition of optical measurement setup



9. RELIABILITY

No.	Test Item	Test Condition	Remark
1	High Temperature Storage	+80℃± 2℃，96 hrs	Note
2	Low Temperature Storage	-30℃± 2℃，96 hrs	Note
3	High Temperature Operation	+70℃± 2℃，96 hrs	Note
4	Low Temperature Operation	+20℃± 2℃，96 hrs	Note
5	High Temperature & High Humidity Storage Test	+50℃± 5℃, 90％R.H, 96 hours	Note
6	Temperature Cycle (non operation)	-30℃ ← +25℃ → +80℃ (30mins ← 5mins →30mins) 10 Cycles	Note
7	Electronic Static Discharge	Air Discharge: 2KV to with 5 times Ambiance: 15℃~35℃,30%~60%R.H Resistance(Rd): 330Ω ±10% Capacitance(Cs + Cd): 150pF±10%	Discharge for each polarity Mode of Operation: Single Discharge, successive discharge at least 1 sec
8	Vibration (Packaged)	Frequency range: 10Hz ~ 55 Hz Amplitude: 1.5mm Direction of X.Y. Z for 3 Hrs in total	
9	Drop Test (Packaged)	Height: 80cm, Time: 1 1 corner, 3 edged, 6 surfaces	

Note : Recovery Time should be 2~4 hours at room temperature (20±8℃) and humidity (below 60% R.H). No abnormalities in functions and appearance