Virtex-II Pro and Virtex-II Pro X Platform FPGAs: Complete Data Sheet

DS083 (v5.0) June 21, 2011

Product Specification

Module 1: Introduction and Overview

10 pages

- Summary of Features
- General Description
- Architecture
- IP Core and Reference Support
- Device/Package Combinations and Maximum I/O
- Ordering Information

Module 2: Functional Description

60 pages

- Functional Description: RocketIO™ X Multi-Gigabit Transceiver
- Functional Description: RocketIO Multi-Gigabit Transceiver
- Functional Description: Processor Block
- Functional Description: PowerPC™ 405 Core
- Functional Description: FPGA
  - Input/Output Blocks (IOBs)
  - Digitally Controlled Impedance (DCI)
  - On-Chip Differential Termination
  - Configurable Logic Blocks (CLBs)
  - 3-State Buffers
  - CLB/Slice Configurations
  - 18-Kb Block SelectRAM™ Resources
  - 18-Bit x 18-Bit Multipliers
  - Global Clock Multiplexer Buffers
  - Digital Clock Manager (DCM)
- Routing
- Configuration

Module 3: DC and Switching Characteristics

59 pages

- Electrical Characteristics
- Performance Characteristics
- Switching Characteristics
- Pin-to-Pin Output Parameter Guidelines
- Pin-to-Pin Input Parameter Guidelines
- DCM Timing Parameters
- Source-Synchronous Switching Characteristics

Module 4: Pinout Information

302 pages

- Pin Definitions
- Pinout Tables
  - FG256/FGG256 Wire-Bond Fine-Pitch BGA Package
  - FG456/FGG456 Wire-Bond Fine-Pitch BGA Package
  - FG676/FGG676 Wire-Bond Fine-Pitch BGA Package
  - FF672 Flip-Chip Fine-Pitch BGA Package
  - FF896 Flip-Chip Fine-Pitch BGA Package
  - FF1148 Flip-Chip Fine-Pitch BGA Package
  - FF1152 Flip-Chip Fine-Pitch BGA Package
  - FF1517 Flip-Chip Fine-Pitch BGA Package
  - FF1696 Flip-Chip Fine-Pitch BGA Package
  - FF1704 Flip-Chip Fine-Pitch BGA Package

IMPORTANT NOTE: *Page, figure, and table numbers begin at 1 for each module, and each module has its own Revision History at the end. Use the PDF "Bookmarks" pane for easy navigation in this volume.*

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Summary of Virtex-II Pro™ / Virtex-II Pro X Features

- High-Performance Platform FPGA Solution, Including
  - Up to twenty RocketIO™ or RocketIO X embedded Multi-Gigabit Transceivers (MGTs)
  - Up to two IBM PowerPC™ RISC processor blocks
- Based on Virtex-II™ Platform FPGA Technology
  - Flexible logic resources
  - SRAM-based in-system configuration
  - Active Interconnect technology
  - SelectRAM™+ memory hierarchy
  - Dedicated 18-bit x 18-bit multiplier blocks
  - High-performance clock management circuitry
  - SelectI/O™-Ultra technology
  - XCITE Digitally Controlled Impedance (DCI) I/O

Virtex-II Pro / Virtex-II Pro X family members and resources are shown in Table 1.

Table 1: **Virtex-II Pro / Virtex-II Pro X FPGA Family Members**

Device[1]	RocketIO Transceiver Blocks	PowerPC Processor Blocks	Logic Cells[2]	CLB (1 = 4 slices = max 128 bits)		18 X 18 Bit Multiplier Blocks	Block SelectRAM+		DCMs	Maximum User I/O Pads
				Slices	Max Distr RAM (Kb)		18 Kb Blocks	Max Block RAM (Kb)		
XC2VP2	4	0	3,168	1,408	44	12	12	216	4	204
XC2VP4	4	1	6,768	3,008	94	28	28	504	4	348
XC2VP7	8	1	11,088	4,928	154	44	44	792	4	396
XC2VP20	8	2	20,880	9,280	290	88	88	1,584	8	564
XC2VPX20	8[4]	1	22,032	9,792	306	88	88	1,584	8	552
XC2VP30	8	2	30,816	13,696	428	136	136	2,448	8	644
XC2VP40	0[3], 8, or 12	2	43,632	19,392	606	192	192	3,456	8	804
XC2VP50	0[3] or 16	2	53,136	23,616	738	232	232	4,176	8	852
XC2VP70	16 or 20	2	74,448	33,088	1,034	328	328	5,904	8	996
XC2VPX70	20[4]	2	74,448	33,088	1,034	308	308	5,544	8	992
XC2VP100	0[3] or 20	2	99,216	44,096	1,378	444	444	7,992	12	1,164

Notes:
1. -7 speed grade devices are not available in Industrial grade.
2. Logic Cell ≈ (1) 4-input LUT + (1)FF + Carry Logic
3. These devices can be ordered in a configuration without RocketIO transceivers. See Table 3 for package configurations.
4. Virtex-II Pro X devices equipped with RocketIO X transceiver cores.

RocketIO X Transceiver Features (XC2VPX20 and XC2VPX70 Only)

- Variable-Speed Full-Duplex Transceiver (XC2VPX20) Allowing 2.488 Gb/s to 6.25 Gb/s Baud Transfer Rates.
  - Includes specific baud rates used by various standards, as listed in Table 4, Module 2.
- Fixed-Speed Full-Duplex Tranceiver (XC2VPX70) Operating at 4.25 Gb/s Baud Transfer Rate.
- Eight or Twenty Transceiver Modules on an FPGA, Depending upon Device
- Monolithic Clock Synthesis and Clock Recovery
  - Eliminates the need for external components
- Automatic Lock-to-Reference Function
- Programmable Serial Output Differential Swing
  - 200 mV to 1600 mV, peak-peak
  - Allows compatibility with other serial system voltage levels
- Programmable Pre-emphasis Levels 0 to 500%
- Telecom/Datacom Support Modes
  - "x8" and "x10" clocking/data paths
  - 64B/66B clocking support