

Module 1: Introduction and Ordering Information

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- Introduction
- Features
- Architectural Overview
- Configuration Overview
- In-system Flash Memory Overview
- General I/O Capabilities
- Supported Packages and Package Marking
- Ordering Information

Module 2: Functional Description

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The functionality of the Spartan®-3AN FPGA family is described in the following documents:

- [UG331: Spartan-3 Generation FPGA User Guide](#)
 - Clocking Resources
 - Digital Clock Managers (DCMs)
 - Block RAM
 - Configurable Logic Blocks (CLBs)
 - Distributed RAM
 - SRL16 Shift Registers
 - Carry and Arithmetic Logic
 - I/O Resources
 - Embedded Multiplier Blocks
 - Programmable Interconnect
 - ISE® Design Tools and IP Cores
 - Embedded Processing and Control Solutions
 - Pin Types and Package Overview
 - Package Drawings
 - Powering FPGAs
 - Power Management
- [UG332: Spartan-3 Generation Configuration User Guide](#)
 - Configuration Overview
 - Configuration Pins and Behavior
 - Bitstream Sizes
 - Detailed Descriptions by Mode
 - Self-contained In-System Flash mode
 - Master Serial Mode using Platform Flash PROM
 - Master SPI Mode using Commodity Serial Flash
 - Master BPI Mode using Commodity Parallel Flash
 - Slave Parallel (SelectMAP) using a Processor
 - Slave Serial using a Processor
 - JTAG Mode
 - ISE iMPACT Programming Examples
 - MultiBoot Reconfiguration
 - Design Authentication using Device DNA
- [UG333: Spartan-3AN In-System Flash User Guide](#)
- [UG334: Spartan-3AN Starter Kit User Guide](#)

Module 3: DC and Switching Characteristics

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- DC Electrical Characteristics
 - Absolute Maximum Ratings
 - Supply Voltage Specifications
 - Recommended Operating Conditions
- Switching Characteristics
 - I/O Timing
 - Configurable Logic Block (CLB) Timing
 - Multiplier Timing
 - Block RAM Timing
 - Digital Clock Manager (DCM) Timing
 - Suspend Mode Timing
 - Device DNA Timing
 - Configuration and JTAG Timing

Module 4: Pinout Descriptions

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- Pin Descriptions
- Package Overview
- Pinout Tables
- Footprint Diagrams

Table 1: Production Status of Spartan-3AN FPGAs

Spartan-3AN FPGA	Status
XC3S50AN	Production
XC3S200AN	Production
XC3S400AN	Production
XC3S700AN	Production
XC3S1400AN	Production

Additional information on the Spartan-3AN family can be found at:

http://www.xilinx.com/support/index.html/content/xilinx/en/supportNav/silicon_devices/fpga/spartan-3an.html.

Introduction

The Spartan®-3AN FPGA family combines the best attributes of a leading edge, low cost FPGA with nonvolatile technology across a broad range of densities. The family combines all the features of the Spartan-3A FPGA family plus leading technology in-system Flash memory for configuration and nonvolatile data storage.

The Spartan-3AN FPGAs are part of the Extended Spartan-3A family, which also includes the Spartan-3A FPGAs and the higher density Spartan-3A DSP FPGAs. The Spartan-3AN FPGA family is excellent for space-constrained applications such as blade servers, medical devices, automotive infotainment, telematics, GPS, and other small consumer products. Combining FPGA and Flash technology minimizes chip count, PCB traces and overall size while increasing system reliability.

The Spartan-3AN FPGA internal configuration interface is completely self-contained, increasing design security. The family maintains full support for external configuration. The Spartan-3AN FPGA is the world's first nonvolatile FPGA with MultiBoot, supporting two or more configuration files in one device, allowing alternative configurations for field upgrades, test modes, or multiple system configurations.

Features

- The new standard for low cost nonvolatile FPGA solutions
- Eliminates traditional nonvolatile FPGA limitations with the advanced 90 nm Spartan-3A device feature set
 - Memory, multipliers, DCMs, SelectIO, hot swap, power management, etc.
- Integrated robust configuration memory
 - Saves board space
 - Improves ease-of-use
 - Simplifies design
 - Reduces support issues
- Plentiful amounts of nonvolatile memory available to the user
 - Up to 11+ Mb available
 - MultiBoot support
 - Embedded processing and code shadowing
 - Scratchpad memory
- Robust 100K Flash memory program/erase cycles
- 20 years Flash memory data retention
- Security features provide bitstream anti-cloning protection
- Buried configuration interface
- Unique Device DNA serial number in each device for design Authentication to prevent unauthorized copying
- Flash memory sector protection and lockdown
- Configuration watchdog timer automatically recovers from configuration errors
- Suspend mode reduces system power consumption
 - Retains all design state and FPGA configuration data
 - Fast response time, typically less than 100 μ s
- Full hot-swap compliance
- Multi-voltage, multi-standard SelectIO™ interface pins
 - Up to 502 I/O pins or 227 differential signal pairs
 - LVCMOS, LVTTTL, HSTL, and SSTL single-ended signal standards
 - 3.3V, 2.5V, 1.8V, 1.5V, and 1.2V signaling
 - Up to 24 mA output drive
 - 3.3V $\pm$ 10% compatibility and hot swap compliance
 - 622+ Mb/s data transfer rate per I/O
 - DDR/DDR2 SDRAM support up to 400 Mb/s
 - LVDS, RSDS, mini-LVDS, PPDS, and HSTL/SSTL differential I/O
- Abundant, flexible logic resources
 - Densities up to 25,344 logic cells
 - Optional shift register or distributed RAM support
 - Enhanced 18 x 18 multipliers with optional pipeline
- Hierarchical SelectRAM™ memory architecture
 - Up to 576 Kbits of dedicated block RAM
 - Up to 176 Kbits of efficient distributed RAM
- Up to eight Digital Clock Managers (DCMs)
- Eight global clocks and eight additional clocks per each half of device, plus abundant low-skew routing
- Complete Xilinx® ISE® and WebPACK™ software development system support
- MicroBlaze™ and PicoBlaze™ embedded processor cores
- Fully compliant 32-/64-bit 33 MHz PCI™ technology support
- Low-cost QFP and BGA Pb-free (RoHS) packaging options
 - Pin-compatible with the same packages in the Spartan-3A FPGA family

Table 2: Summary of Spartan-3AN FPGA Attributes

Device	System Gates	Equivalent Logic Cells	CLBs	Slices	Distributed RAM Bits ⁽¹⁾	Block RAM Bits ⁽¹⁾	Dedicated Multipliers	DCMs	Maximum User I/O	Max Differential I/O Pairs	Bitstream Size ⁽¹⁾	In-System Flash Bits
XC3S50AN	50K	1,584	176	704	11K	54K	3	2	108	50	427K	1M ⁽²⁾
XC3S200AN	200K	4,032	448	1,792	28K	288K	16	4	195	90	1,168K	4M
XC3S400AN	400K	8,064	896	3,584	56K	360K	20	4	311	142	1,842K	4M
XC3S700AN	700K	13,248	1,472	5,888	92K	360K	20	8	372	165	2,669K	8M
XC3S1400AN	1400K	25,344	2,816	11,264	176K	576K	32	8	502	227	4,644K	16M

Notes:

1. By convention, one Kb is equivalent to 1,024 bits and one Mb is equivalent to 1,024 Kb.
2. Maximum supported by Xilinx tools. See the customer notice [XCIN14003: Flash Wafer Fabrication Change and Gold \(Au\) To Copper \(Cu\) Transition for Spartan-3AN FPGA Devices](#).