

TITLE:**DV320FHM-NN0 Product Specification**

BEIJING BOE DISPLAY TECHNOLOGY

SPEC. NUMBER
S8XX-XXXXPRODUCT GROUP
TFT LCDREV.
P0ISSUE DATE
2016.04.07PAGE
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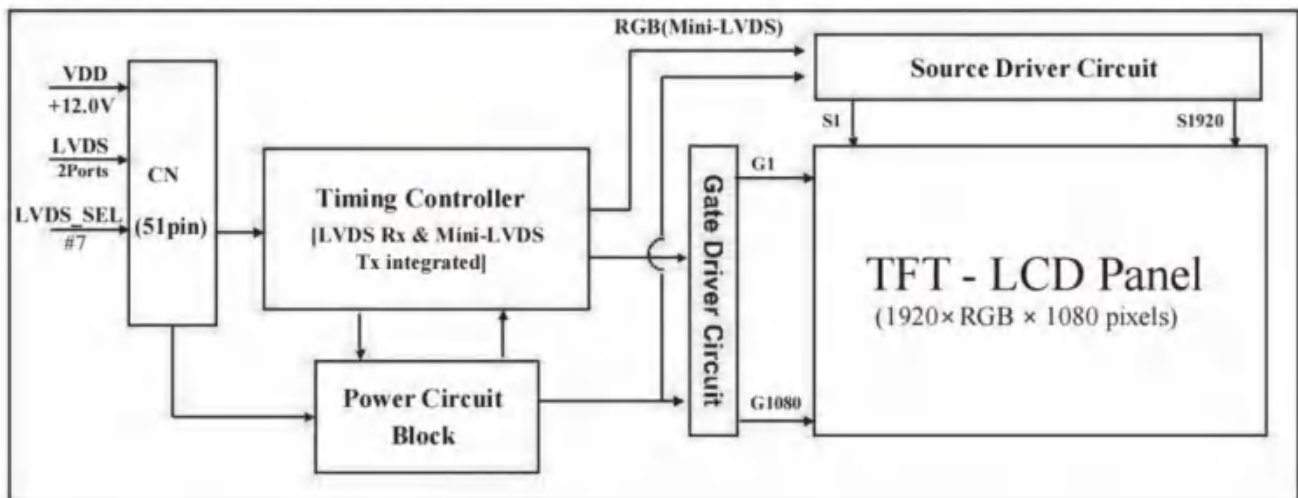
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1.0 GENERAL DESCRIPTION

1.1 Introduction

DV320FHM-NN0 is a color active matrix TFT LCD MDL using amorphous silicon TFT's (Thin Film Transistors) as an active switching devices. This open cell has a 31.51 inch diagonally measured active area with FHD resolutions (1920 horizontal by 1080 vertical pixel array). Each pixel is divided into RED, GREEN, BLUE dots which are arranged in vertical stripe and this open cell can display 16.7M colors. The TFT-LCD panel used for this open cell is adapted for a low reflection and higher color type.



1.2 Features

- LVDS interface with 2 pixel / clock
- High-speed response
- Low color shift image quality
- 8-bit color depth, display 16.7M colors
- High luminance and contrast ratio, low reflection and wide viewing angle
- DE (Data Enable) only mode
- ADSDS technology is applied for high display quality
- RoHS compliant

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1.3 Application

- Home Alone Multimedia TFT-LCD TV
- Display Terminals for Control System
- High Definition TV(FHD TV)
- AV application Products

1.4 General Specification

< Table 1. General Specifications >

Parameter	Specification	Unit	Remark
Active area	698.4(H) × 392.85 (V)	mm	
Number of pixels	1920(H)×1080(V)	pixels	
Pixel pitch	121.25(H)×RGB×363.75(V)	μm	
Pixel arrangement	Pixels RGB Vertical stripe		
Display colors	16.7M(8bits-true)	colors	
Display mode	Transmission mode, Normally Black		
Open Cell Transmittance	5.0 (Typ.)	%	At center point with BOE BLU
Weight	4.2(Typ)	Kg	
Power Consumption	4.0	Watt	
Surface Treatment	Haze 1%		

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2.0 ABSOLUTE MAXIMUM RATINGS

The followings are maximum values which, if exceed, may cause faulty operation or damage to the unit. The operational and non-operational maximum voltage and current values are listed in Table 2.

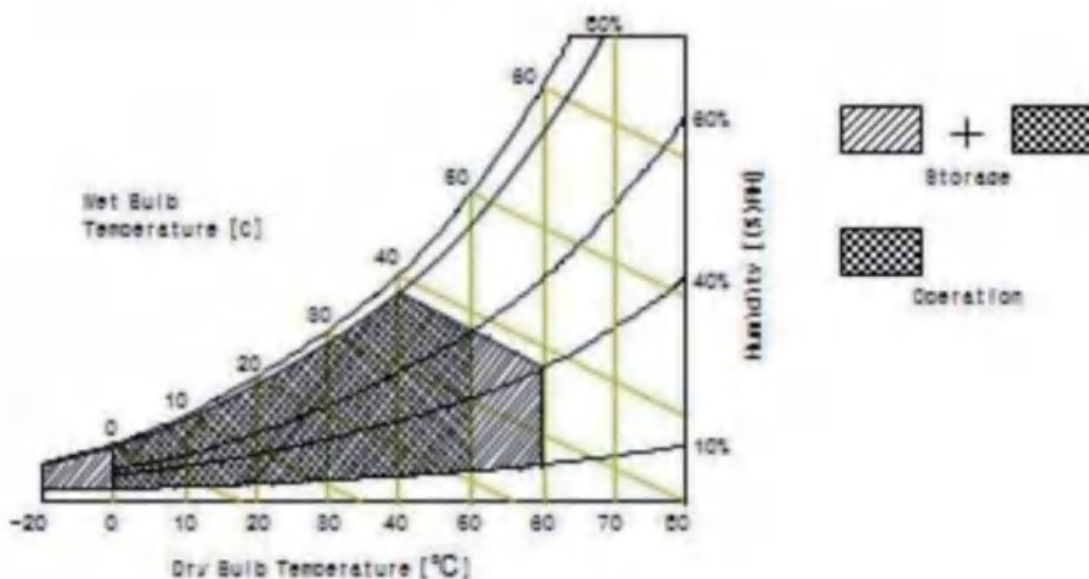
< Table 2. Open Cell Electrical Specifications >

[VSS=GND=0V]

Parameter	Symbol	Min.	Max.	Unit	Remark
Power Supply Voltage	VDD	VSS-0.3	13.2	V	Ta = 25°C
Operating Temperature	T _{OP}	0	+50	°C	Note 1
	T _{SUR}	0	+60	°C	
Storage Temperature	T _{ST}	-20	+60	°C	
Operating Ambient Humidity	H _{OP}	10	80	%RH	
Storage Humidity	H _{ST}	10	80	%RH	

Note 1 : Temperature and relative humidity range are shown in the figure below.

Wet bulb temperature should be 39 °C max. and no condensation of water.



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3.0 ELECTRICAL SPECIFICATIONS

3.1 TFT LCD Open Cell

< Table 3. Open Cell Electrical Specifications >

[Ta=25±2°C]

Parameter		Symbol	Values			Unit	Remark
			Min	Typ	Max		
Power Supply Input Voltage		VDD	10.8	12	13.2	Vdc	
Power Supply Ripple Voltage		VRP			300	mV	
Power Supply Current		IDD	-	333	630	mA	Note 1
Power Consumption		PDD		4.0	7.6	Watt	
Rush current		IRUSH	-	-	3.0	A	Note 2
LVDS Interface	Differential Input High Threshold Voltage	VLVTH	+100		+300	mV	
	Differential Input Low Threshold Voltage	VLVTL	-300		-100	mV	
	Common Input Voltage	VLVC	1.0	1.2	1.4	V	
CMOS Interface	Input High Threshold Voltage	VIH	2.7	-	3.3	V	
	Input Low Threshold Voltage	VIL	0	-	0.6	V	

Note 1 : The supply voltage is measured and specified at the interface connector of LCM.

The current draw and power consumption specified is for VDD=12.0V,

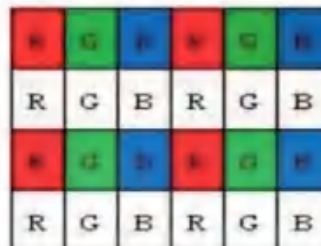
Frame rate $f_v=60\text{Hz}$ and Clock frequency = 75.4MHz.

Test Pattern of power supply current

a) Typ : Mosaic 8 x 6 Pattern(L0/L255)
Pattern(L0/L255)



b) Max : H- Stripe



Note 2 : The duration of rush current is about 2ms and rising time of Power Input is 1ms(min)

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3.2 LED Converter

3.2.1 Input Electrical Characteristics :

INPUT VOLTAGE :

Minimum	Nominal	Maximum	Unit
24V/2.0A	24V/2.5A	-	V/A

3.2.2 Output Electrical Characteristics :

DC OUTPUT :

LED DRIVER (DC/DC) ELECTRICAL REQUIREMENTS:

Notes: The LED protection test for a single set of test.

a.LIGHT BAR TYPE:

LTEM	DESCRIPTION	CONDITION	MIN.	TYP	MAX	UNIT
1	LED VOLTAGE		84	90	96	Vdc
2	LED CURRENT		-	480	-	mA
3		DEVIATION		5		%
4	POWER CONSUMPTION		-	-	46	W
5	BACKLINHT ON/OFF CONTROL	ON	2.5		5	Vdc
		OFF	0		0.7	HZ
6	DC/PWM DIMMING	Frequency	100		200	HZ
		Duty cycle	20		100	%

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Notes: When the discrepancy of lights voltage is more than 3.0V, Please do not use the LED driver.

a. Protection characteristics:

ITEM	CONDITION	SPECIFICATION
1.LED OPEN PROTECTION:	OPEN OUTPUT	SHUTDOWN AND NO DAMAGE
2.LED STRING SHORT PROTECTION:	SHORT OUTPUT	SHUTDOWN AND NO DAMAGE

Mechanical Characteristics :

3.3 Dimension:

106.0(L)*73.0(W)*13(H) mm (L *W * H)



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3.4 CN1-14PIN-2.0

Pin No	Symbol	Description	
1	VBL	Power Supply +24V	
2	VBL	Power Supply +24V	
3	VBL	Power Supply +24V	
4	VBL	Power Supply +24V	
5	VBL	Power Supply +24V	
6	GND	Ground	
7	GND	Ground	
8	GND	Ground	
9	GND	Ground	
10	GND	Ground	
11	NC	No Connection	
12	VBLOFF	BLU On-Off control	Max : 3.3V / Min : 0V
13	PWM 调光	0V:Min, 3.3V:Max	On : 2.8V~5.0V/Off :0~0.8V
14	NC	NC	

While system is turned ON or OFF, the power sequences must follow as below descriptions:

Turn ON sequence: VBL-ON → PWM signal → BLON

Turn OFF sequence: BLOFF → PWM signal → VBL-ON

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4.0 INTERFACE CONNECTION

4.1 Module Input Signal & Power

- Connector : IS050-C51B-C39-S (UJU) / FI-RE51S-HF-R1500 (JAE) or Equivalent.

< Table 4. Open Cell Input Connector Pin Configuration >

Pin No	Symbol	Description	Pin No	Symbol	Description
1	NC	No Connection	21	GND	Ground
2	SDA	I ² C Data	22	CH1[3]-	First pixel negative LVDS differential data input. Pair3
3	SCL	I ² C Clock	23	CH1[3]+	First pixel positive LVDS differential data input. Pair3
4	NC	Not Connected	24	NC	Not Connected
5	NC	Not Connected	25	NC	Not Connected
6	NC	Not Connected	26	NC	Not Connected
7	SELLVDS	High: JEIDA Low or Open: VESA	27	NC	Not Connected
8	NC	Not Connected	28	CH2[0]-	Second pixel negative LVDS differential data input. Pair0
9	NC	Not Connected	29	CH2[0]+	Second pixel positive LVDS differential data input. Pair0
10	NC	Not Connected	30	CH2[1]-	Second pixel negative LVDS differential data input. Pair1
11	GND	Ground	31	CH2[1]+	Second pixel positive LVDS differential data input. Pair1
12	CH1[0]-	First pixel negative LVDS differential data input. Pair0	32	CH2[2]-	Second pixel negative LVDS differential data input. Pair2
13	CH1[0]+	First pixel positive LVDS differential data input. Pair0	33	CH2[2]+	Second pixel positive LVDS differential data input. Pair2
14	CH1[1]-	First pixel negative LVDS differential data input. Pair1	34	GND	Ground
15	CH1[1]+	First pixel positive LVDS differential data input. Pair1	35	CH2CLK-	Second pixel negative LVDS clock
16	CH1[2]-	First pixel negative LVDS differential data input. Pair2	36	CH2CLK+	Second pixel positive LVDS clock
17	CH1[2]+	First pixel positive LVDS differential data input. Pair2	37	GND	Ground
18	GND	Ground	38	CH2[3]-	Second pixel negative LVDS differential data input. Pair3
19	CH1CLK-	First pixel negative LVDS clock	39	CH2[3]+	Second pixel positive LVDS differential data input. Pair3
20	CH1CLK+	First pixel positive LVDS clock			

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Pin No	Symbol	Description	Pin No	Symbol	Description
40	NC	Not Connected	46	GND	Ground
41	NC	Not Connected	47	NC	Not Connected
42	NC	Not Connected	48	VCC	Input Voltage +12V
43	NC	Not Connected	49	VCC	Input Voltage +12V
44	GND	Ground	50	VCC	Input Voltage +12V
45	GND	Ground	51	VCC	Input Voltage +12V

Notes : 1. NC(Not Connected) : This pins are only used for BOE internal operations.

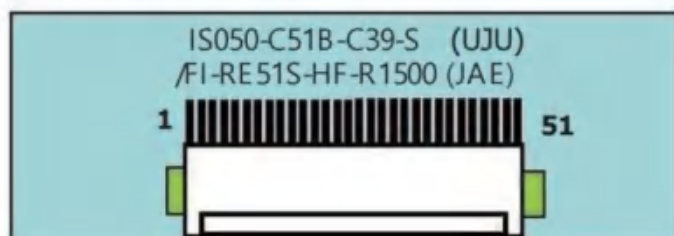
2. Input Level of LVDS signal is based on the IEA 664 Standard.

3. LVDS_SEL : This pin is used for selecting LVDS signal data format.

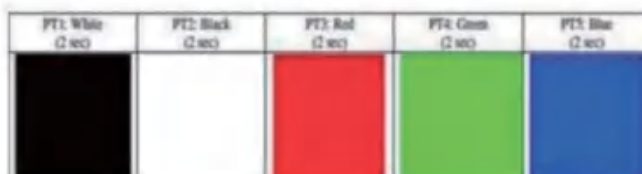
If this Pin : High (3.3V) → JEIDA LVDS format

Otherwise : Low (GND) or Open (NC) → Normal NS LVDS format

Rear view of LCM



BIST Pattern



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