

Product Specification

Part Name: OEL Display Moudle
Customer Part ID:
LiYuan Electronics Part ID: LY078X2880TSWKG01H13
Ver: A

Customer:
Approved by

From: LiYuan Electronics Co.,Ltd.
Approved by

LiYuan Electronics Co.,Ltd.

- Notes:
- 1. Please contact LiYuan Electronics before assigning your product based on this module specification
 - 2. The information contained herein is presented merely to indicate the characteristics and performance of our products. No responsibility is assumed by LiYuan Electronics for any intellectual property claims or other problems that may result from application based on the module described herein.

Revised History

Part Number	Revision	Revision Content	Revised on
LY078X2880TSWKG01H13	A	New	20190522

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Revision History

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1. Basic Specifications

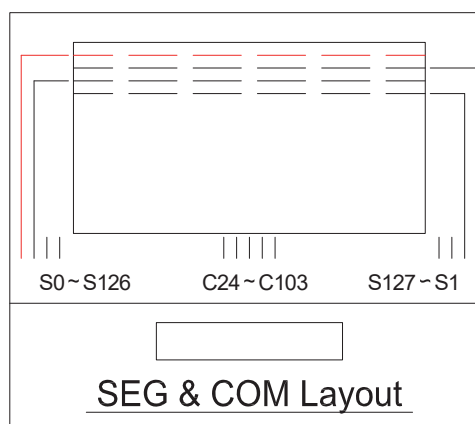
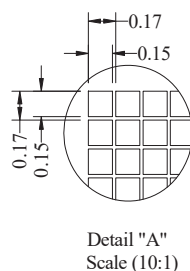
1.1 Display Specifications

- | | |
|-------------------|--------------------|
| 1) Display Mode: | Passive Matrix |
| 2) Display Color: | Monochrome (White) |
| 3) Drive Duty: | 1/80 Duty |

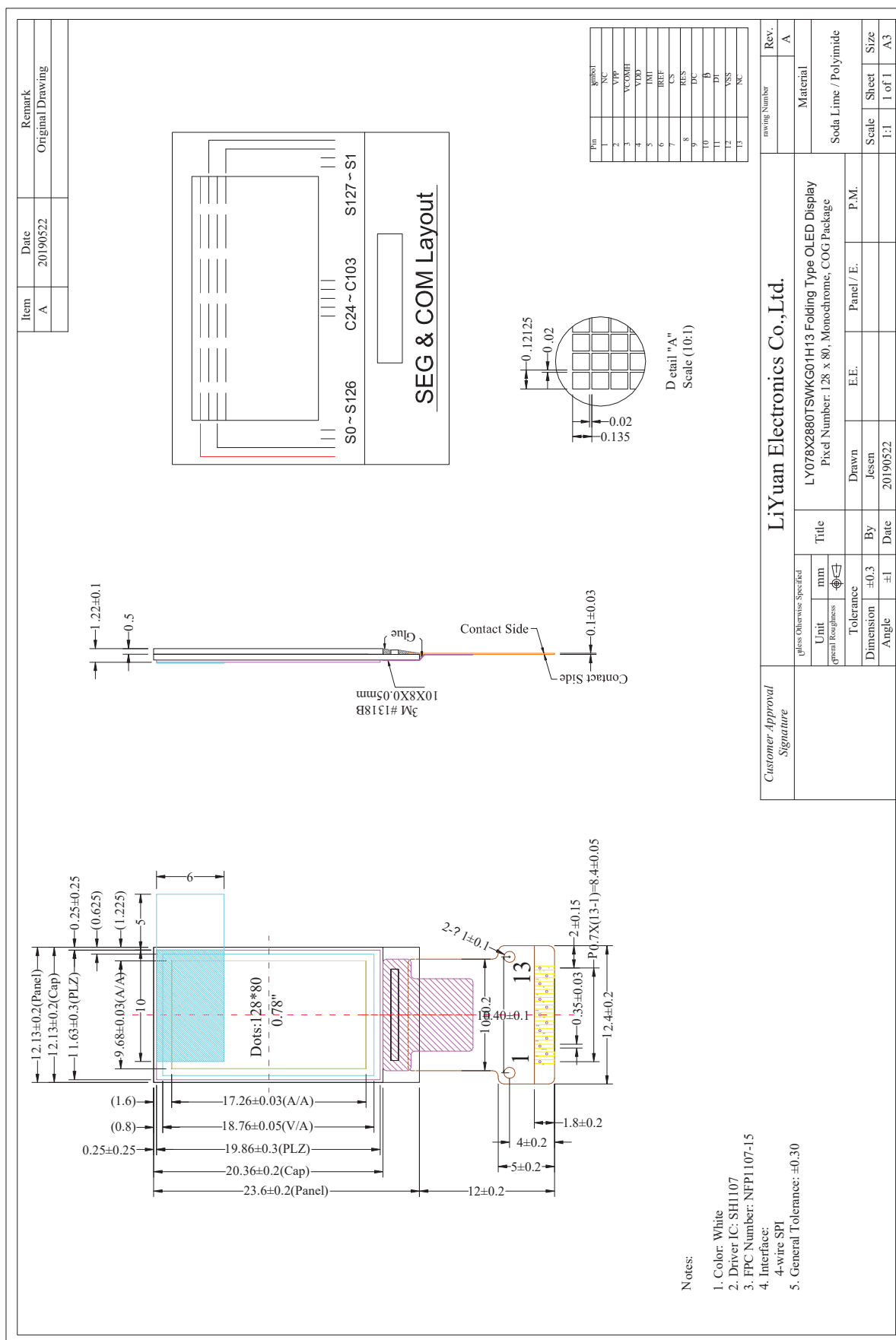
1.2 Mechanical Specifications

- | | |
|----------------------|--|
| 1) Outline Drawing: | According to the annexed outline drawing |
| 2) Number of Pixels: | 128 × 80 |
| 3) Panel Size: | 12.13 × 23.6 × 1.22 (mm) |
| 4) Active Area: | 9.68 × 17.26 (mm) |
| 5) Pixel Pitch: | 0.17 × 0.17 (mm) |
| 6) Pixel Size: | 0.15 × 0.15 (mm) |
| 7) Weight: | TBD |

1.3 Active Area / Memory Mapping & Pixel Construction



1.4 Mechanical Drawing



1.5 Pin Definition

Pin Number	Symbol	I/O	Function						
Power Supply									
2	VPP	P	power Supply for OEL Panell This is the most positive voltage supply pin of the chip. It must be supplied externally.						
4	VDD	P	Power Supply for Logic This is a voltage supply pin. It must be connected to external source.						
12	VSS	P	Ground of OEL System This is a ground pin. It also acts as a reference for the logic pins, the OEL driving voltages, and the analog circuits. It must be connected to external ground.						
Driver									
6	IREF	I	Current Reference for Brightness Adjustment This pin is segment current reference pin. A resistor should be connected between this pin and V _{SS} . Set the current at 12.5μA maximum.						
3	VCOMH	O	Voltage Output High Level for COM Signal This pin is the input pin for the voltage output high level for COM signals. A capacitor should be connected between this pin and V _{SS} .						
Interface									
5	IM1	I	Communicating Protocol Select These pins are MCU interface selection input. See the following table: <table><tr><td></td><td>IM1</td></tr><tr><td>4-wire SPI</td><td>0</td></tr><tr><td>I₂C</td><td>1</td></tr></table>		IM1	4-wire SPI	0	I ₂ C	1
	IM1								
4-wire SPI	0								
I ₂ C	1								
8	RES#	I	Power Reset for Controller and Driver This pin is reset signal input. When the pin is low, initialization of the chip is executed. Keep this pin pull high during normal operation.						
7	CS#	I	Chip Select This pin is the chip select input. The chip is enabled for MCU communication only when CS# is pulled low.						
9	A0	I	Data/Command Control This pin is Data/Command control pin. When the pin is pulled high, the input at D7~D0 will be interpreted as display data. When the pin is pulled low, the input at D7~D0 will be transferred to the command register. When the pin is pulled high and serial interface mode is selected, the data at SI will be interpreted as data. When it is pulled low, the data at SI will be transferred to the command register. In I ₂ C mode, this pin acts as SA0 for slave address selection. For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams.						
10,11	D0,D1	I/O	Serial Data Input/Output and clock When serial mode is selected, D1 will be the serial data input SI and D0 will be the serial clock input SCL. When I ₂ C mode is selected, D1 be the serial data input SDA and D0 is the serial clock input, SCL.						
Reserve									
1,13	NC	-	Reserved Pin The N.C. pins between function pins are reserved for compatible and flexible design.						

2. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Notes
Supply Voltage for Logic	V_{DD}	-0.3	3.6	V	1, 2
Supply Voltage for Display	V_{PP}	7	16.5	V	1, 2
Operating Temperature	T_{Op}	-40	70	°C	
Storage Temperature	T_{STG}	-40	85	°C	3
Life Time (150 cd/m ²)		10,000	-	hour	4

Note 1: All the above voltages are on the basis of " $V_{SS} = 0V$ ".

Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. Also, for normal operations, it is desirable to use this module under the conditions according to Section 3. "Optics & Electrical Characteristics". If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate.

Note 3: The defined temperature ranges do not include the polarizer. The maximum withstood temperature of the polarizer should be 80°C.

Note 4: End of lifetime is specified as 50% of initial brightness reached. The reference average operation life time at room temperature is estimated by the accelerated at high temperature conditions.

3. Optics & Electrical Characteristics

3.1 Optics Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Brightness (V _{PP} Supplied Externally)	L _{br}	Note 4	170	220	-	cd/m ²
C.I.E. (White)	(x) (y)	C.I.E. 1931	0.25 0.27	0.29 0.31	0.33 0.35	
Dark Room Contrast	CR		-	>10000:1	-	
Viewing Angle			-	Free	-	degree

* Optical measurement taken at V_{DD} = 2.8V, V_{PP} = 9V.
Software configuration follows Section 4.5 Initialization.

3.2 DC Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage for Logic	V _{DD}		1.65	2.8	3.5	V
Supply Voltage for Display	V _{PP}	Note 5	8.5	9.0	9.5	V
High Level Input	V _{IH}	I _{OUT} = 100μA, 3.3MHz	0.8×V _{DD}	-	V _{DD}	V
Low Level Input	V _{IL}	I _{OUT} = 100μA, 3.3MHz	0	-	0.2×V _{DD}	V
High Level Output	V _{OH}	I _{OUT} = 100μA, 3.3MHz	0.8×V _{DD}	-	V _{DD}	V
Low Level Output	V _{OL}	I _{OUT} = 100μA, 3.3MHz	0	-	0.2×V _{DD}	V
Operating Current for V _{CI}	I _{DD}		-	55	100	μA
Operating Current for V _{PP}	I _{PP}	Note 6	-	13	18	mA
Sleep Mode Current for V _{DD}	I _{DD, SLEEP}		-	0.1	5	μA
Sleep Mode Current for V _{PP}	I _{PP, SLEEP}		-	0.5	5	μA

Note 5 & 6: Brightness (L_{br}) and Supply Voltage for Display (V_{PP}) are subject to the change of the panel characteristics and the customer's request.

Note 6: V_{DD} = 2.8V, V_{PP} = 9.0V, 100% Display Area Turn on.

* Software configuration follows Section 4.5 Initialization.

3.3 AC Characteristics

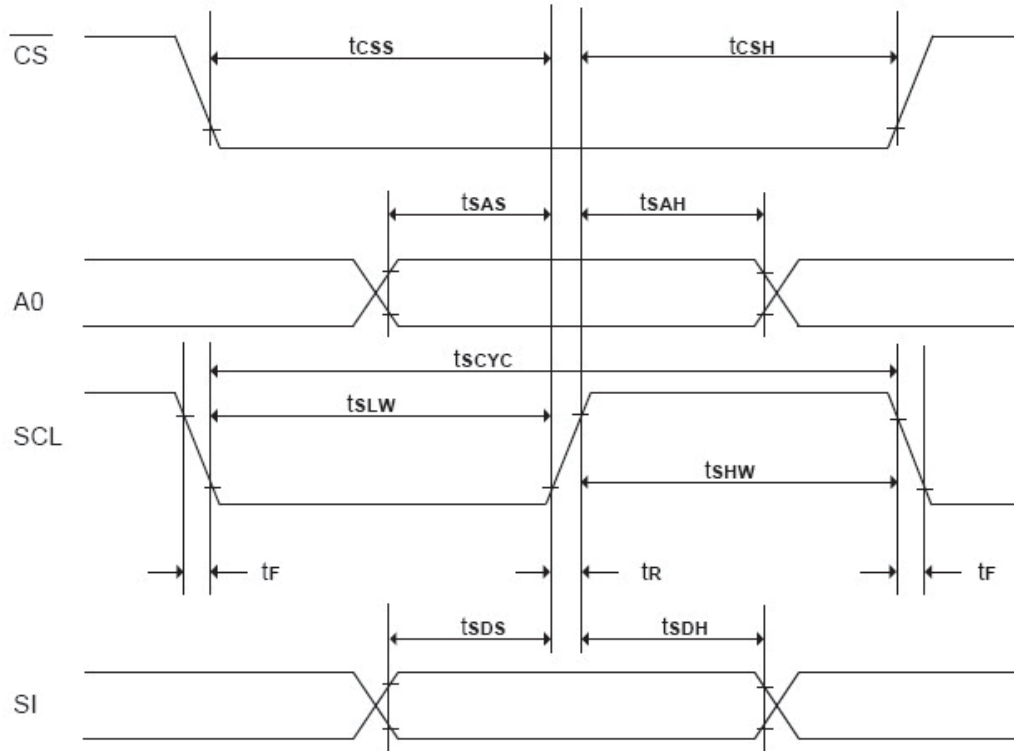
3.3.3.1 Serial Interface Timing Characteristics: (4-wire SPI)

($V_{DD} - V_{SS} = 1.65V$ to $2.4V$, $T_a = 25^{\circ}C$)

Symbol	Description	Min	Max	Unit
t_{SCYC}	Serial Clock Cycle Time	500	-	ns
t_{SAS}	Address Setup Time	300	-	ns
t_{SAH}	Address Hold Time	300	-	ns
t_{SDS}	Data Setup Time	200	-	ns
t_{SDH}	Data Hold Time	200	-	ns
t_{CSS}	Chip Select Setup Time	240	-	ns
t_{CSH}	Chip Select Hold Time	120	-	ns
t_{SHW}	Serial Clock H Pulse Width	200	-	ns
t_{SLW}	Serial Clock L Pulse Width	200	-	ns
t_R	Rise Time	-	30	ns
t_F	Fall Time	-	30	ns

($V_{DD} - V_{SS} = 2.4V$ to $3.5V$, $T_a = 25^{\circ}C$)

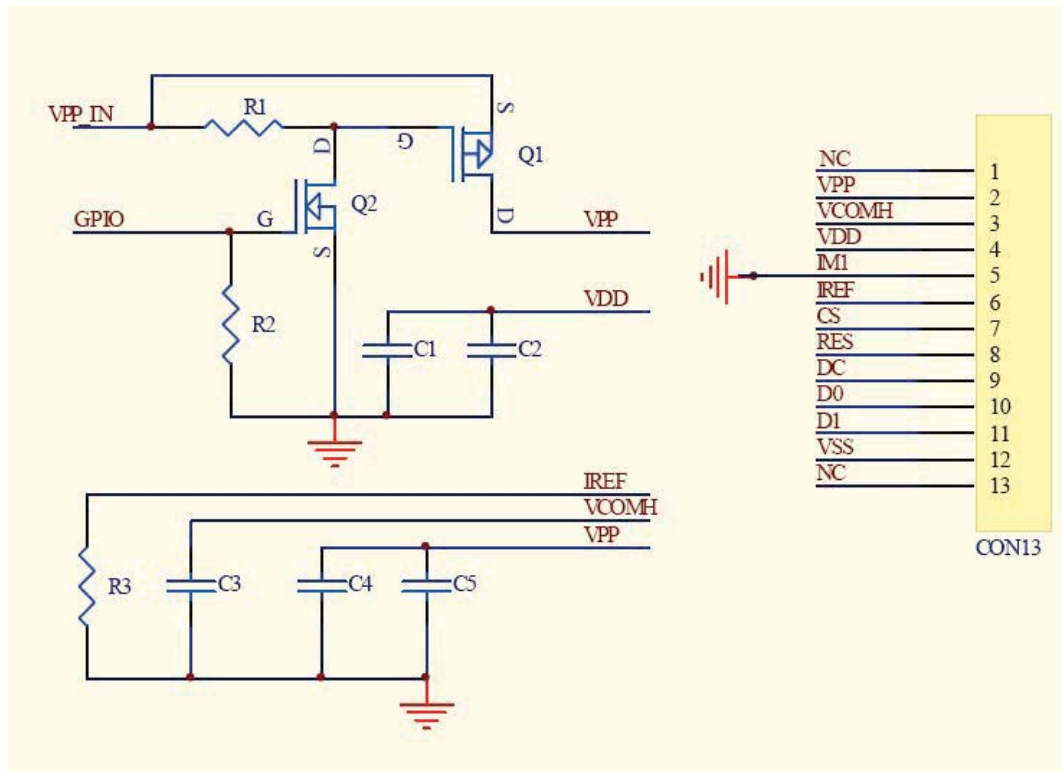
Symbol	Description	Min	Max	Unit
t_{SCYC}	Serial Clock Cycle Time	250	-	ns
t_{SAS}	Address Setup Time	150	-	ns
t_{SAH}	Address Hold Time	150	-	ns
t_{SDS}	Data Setup Time	100	-	ns
t_{SDH}	Data Hold Time	100	-	ns
t_{CSS}	Chip Select Setup Time	120	-	ns
t_{CSH}	Chip Select Hold Time	60	-	ns
t_{SHW}	Serial Clock H Pulse Width	100	-	ns
t_{SLW}	Serial Clock L Pulse Width	100	-	ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns



3.3.3.2 4-wire Serial Interface

特别提醒(Special Tips): 主板设计务必加电子开关, 否则, 可能引起漏电流现象

(When design main board, Please add Electronic Switch circuit, otherwise, will be caused leak current)



Recommended Components:

C1,:	0.1μF / 6.3V, X5R
C2:	4.7μF / 6.3V, X5R
C3:	2.2μF/ 16V, X7R
C4:	4.7μF / 16V, X7R
C5:	0.1μF / 16V, X7R
R3:	560KΩ, $R3 = (\text{Voltage at IREF} - \text{VSS}) / \text{IREF}$
R2, R1:	47kΩ
Q1:	FDN338P
Q2:	FDN335N

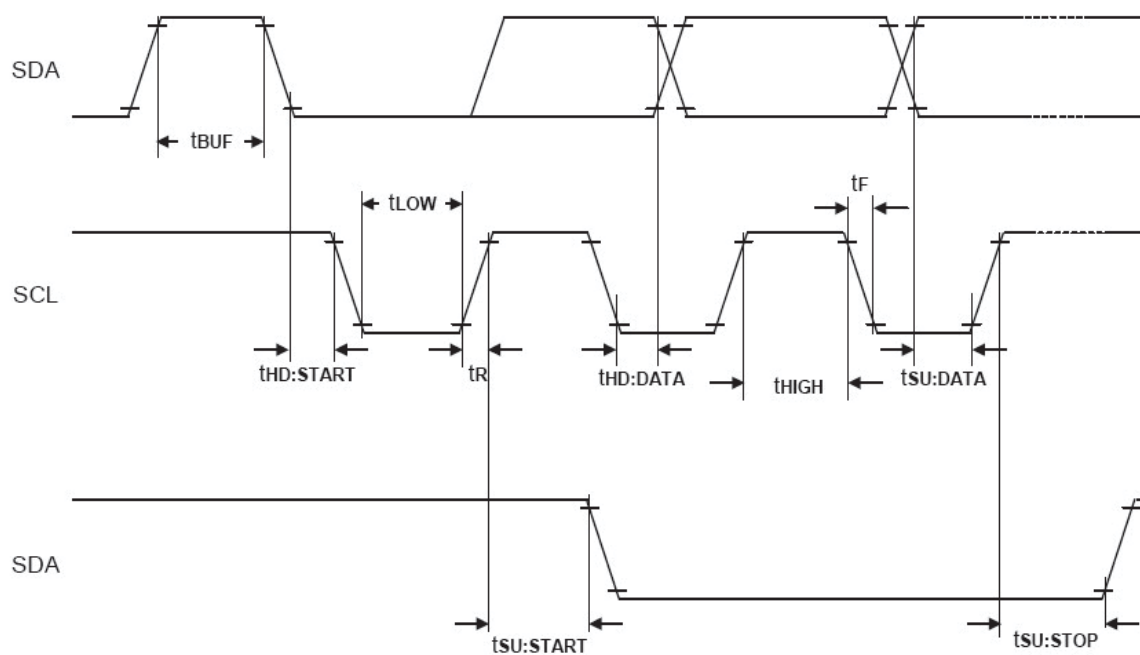
Notes:

VDD:	1.65~3.5V, it should be equal to MPU I/O voltage.
Vpp_in:	8.5~9.5V

3.3.4.1 I2C Interface Timing Characteristics:

($V_{DD} = 1.65 - 3.5V$, $T_A = +25^{\circ}C$)

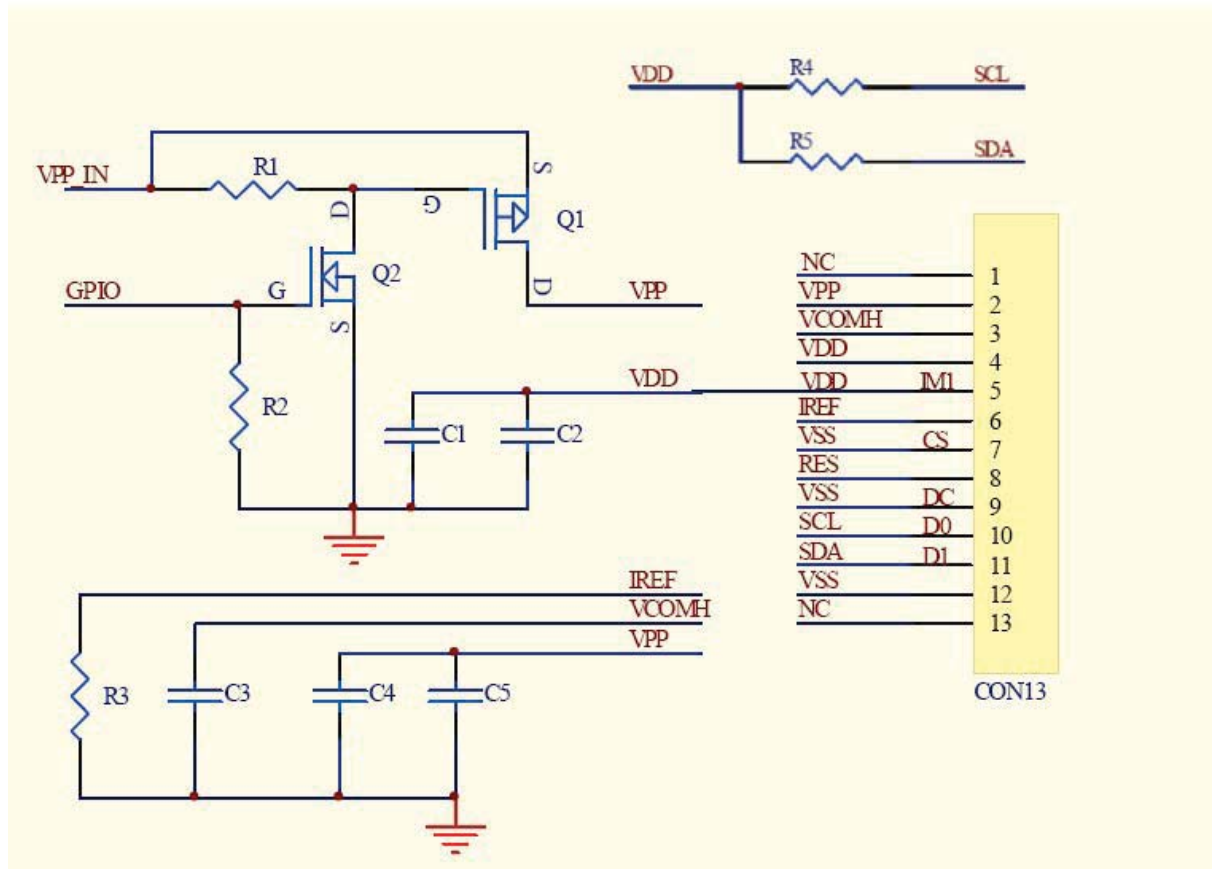
Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
fSCL	SCL clock frequency	DC	-	400	kHz	
TLOW	SCL clock Low pulse width	1.3	-	-	μs	
THIGH	SCL clock H pulse width	0.6	-	-	μs	
TSU:DATA	data setup time	100	-	-	ns	
THD:DATA	data hold time	0	-	0.9	μs	
TR	SCL, SDA rise time	$20+0.1C_b$	-	300	ns	
TF	SCL, SDA fall time	$20+0.1C_b$	-	300	ns	
Cb	Capacity load on each bus line	-	-	400	pF	
TSU:START	Setup time for re-START	0.6	-	-	μs	
THD:START	START Hold time	0.6	-	-	μs	
TSU:STOP	Setup time for STOP	0.6	-	-	μs	
TBUF	Bus free times between STOP and START condition	1.3	-	-	μs	



3.3.4.2 I²C Interface Characteristics

特别提醒(Special Tips): 主板设计务必加电子开关, 否则, 可能引起漏电流现象

(When design main board, Please add Electronic Switch circuit, otherwise, will be caused leak current)



Recommended Components:

- C1,: 0.1μF / 6.3V, X5R
- C2: 4.7μF / 6.3V, X5R
- C3: 4.7μF / 16V, X7R
- C4: 4.7μF / 16V, X7R
- C5: 0.1μF / 16V, X7R
- R3: 560KΩ, $R3 = (\text{Voltage at IREF} - \text{VSS}) / \text{IREF}$
- R2, R1: 47kΩ
- R4, R5 : 4.7 kΩ
- Q1: FDN338P
- Q2: FDN335N

Notes:

- VDD: 1.65~3.5V, it should be equal to MPU I/O voltage.
- Vpp_in: 8.5~9.5V

4. Functional Specification

4.1 Commands

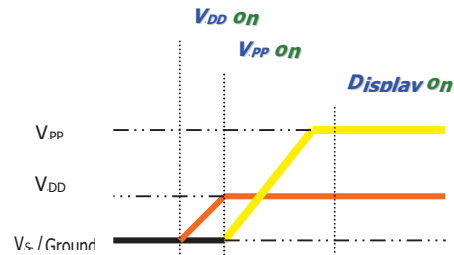
Refer to the Technical Manual for the SH1107

4.2 Power down and Power up Sequence

To protect OEL panel and extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. It gives the OEL panel enough time to complete the action of charge and discharge before/after the operation.

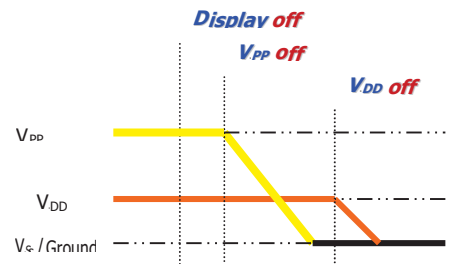
4.2.1 Power up Sequence:

1. Power up VDD
2. Send Display off command
3. Initialization
4. Clear Screen
5. Power up VPP
6. Delay 100ms
(When VPP is stable)
7. Send Display on command



4.2.2 Power down Sequence:

1. Send Display off command
2. Power down VPP
3. Delay 100ms
(When VPP is reach 0 and panel is completely discharges)
4. Power down VDD



Note 9:

- 1) Since an ESD protection circuit is connected between VDD and VBPPB inside the driver IC, VPP becomes lower than VDD whenever VBDDDB is ON and VPP is OFF.
- 2) VPPB should be kept float (disable) when it is OFF.
- 3) Power Pins (VDD, VPP) can never be pulled to ground under any circumstance.
- 4) VBDDDB should not be power down before VPP power down.

4.3 Reset Circuit

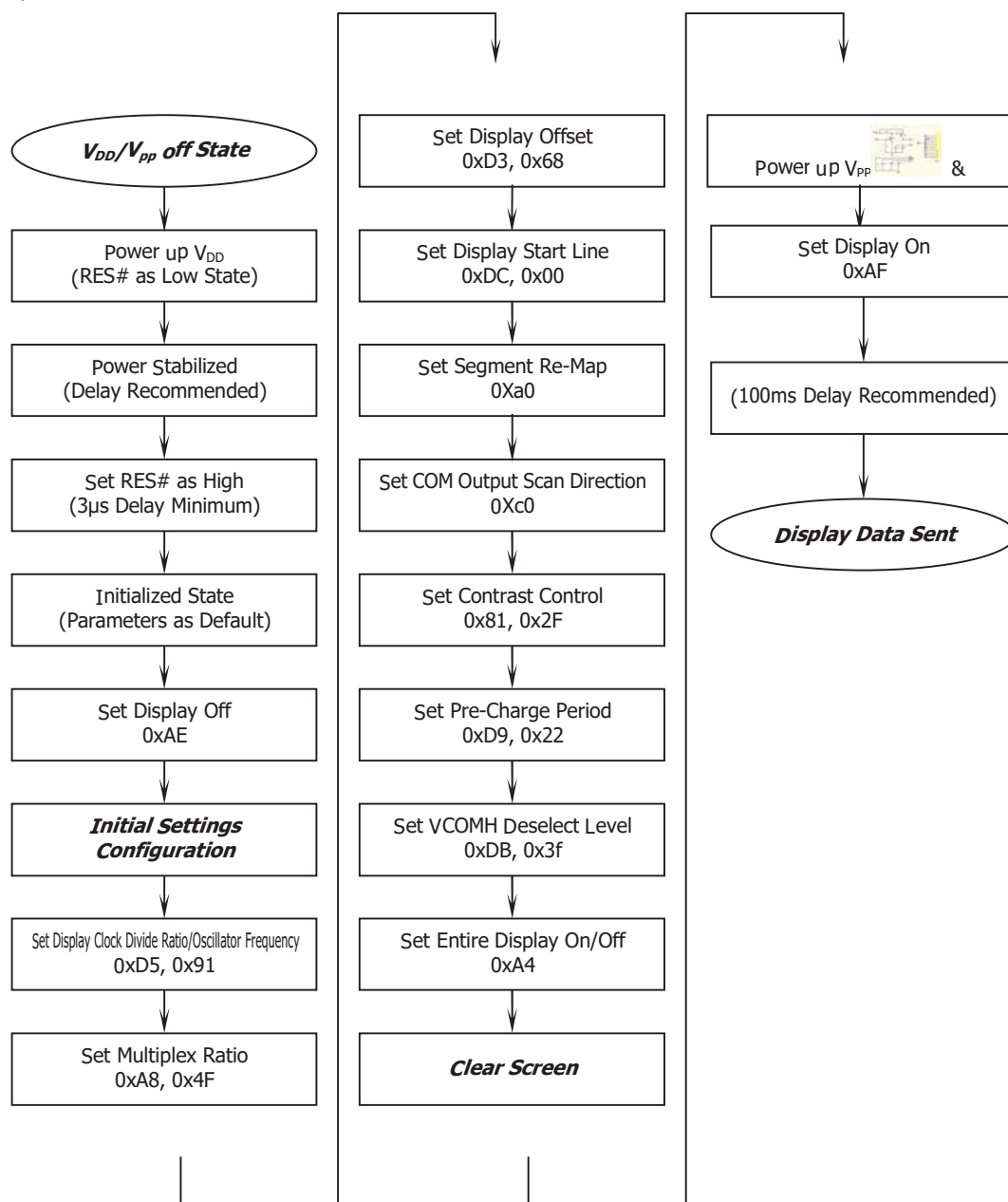
When RESB input is low, the chip is initialized with the following status:

1. Display is OFF. Common and Segment are in high impedance state.
2. 128'128 Display Mode
3. Normal segment and display data column and row address mapping (SEG0 is mapped to the top line of the display).
4. Shift register data clear in serial interface
5. Column address counter is set at 0
6. Normal scan direction of the COM outputs
7. Contrast control register is set at 80h
8. Internal DC-DC is selected

4.4 Actual Application Example

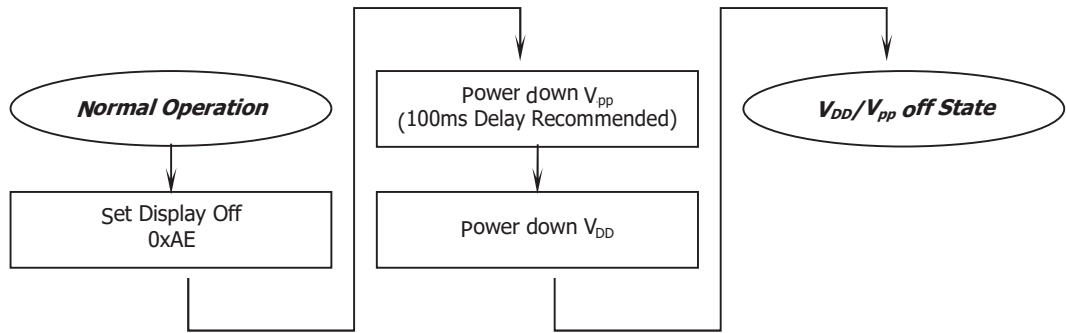
Command usage and explanation of an actual example

4.4.1 V_{DD} Supplied Externally

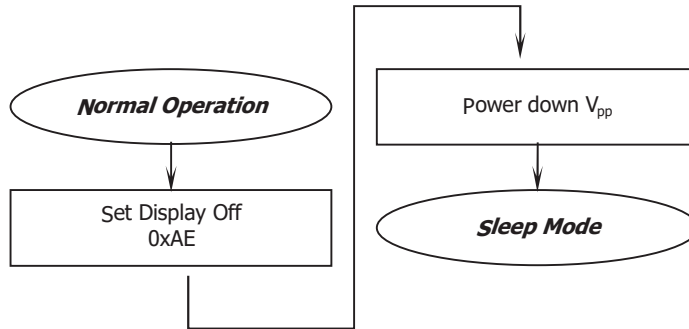


If the noise is accidentally occurred at the displaying window during the operation, please reset the display in order to recover the display function.

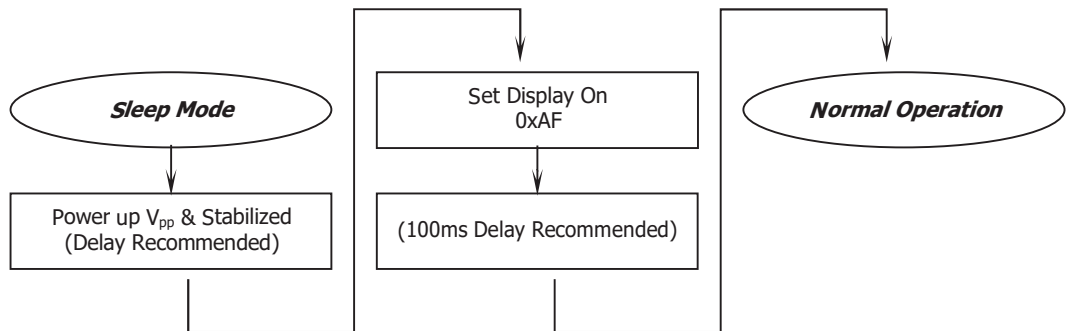
<Power down Sequence>



<Entering Sleep Mode>



<Exiting Sleep Mode>



External setting
void sh1107()

```

{
    write_i(0xAE);    /*display off*/

    write_i(0x00);    /*set lower column address*/
    write_i(0x10);    /*set higher column address*/

    write_i(0x20);    /* Set Memory addressing mode (0x20/0x21) */

    write_i(0x81);    /*contract control*/
    write_i(0x2f);    /*b0*/

    write_i(0xA0);    /*set segment remap*/

    write_i(0xC0);    /*Com scan direction*/
  
```



```
write_i(0xA4);    /*Disable Entire Display On (0xA4/0xA5)*/  
  
write_i(0xA6);    /*normal / reverse*/  
  
write_i(0xD5);    /*set osc division*/  
write_i(0x91);  
  
write_i(0xD9);    /*set pre-charge period*/  
write_i(0x22);  
  
write_i(0xdb);    /*set vcomh*/  
write_i(0x3f);  
  
write_i(0xA8);    /*multiplex ratio*/  
write_i(0x4F);    /*duty = 1/80*/  
  
write_i(0xD3);    /*set display offset*/  
write_i(0x68);    /*18*/  
  
write_i(0xdc);    /*Set Display Start Line*/  
write_i(0x00);  
  
write_i(0xad);    /*set charge pump enable*/  
write_i(0x8a);    /*Set DC-DC enable (a=0:disable; a=1:enable) */  
  
write_i(0xAF);    /*display ON*/  
  
}
```

5. Reliability

5.1 Contents of Reliability Tests

Item	Conditions	Criteria
High Temperature Operation	70°C, 240 hrs	The operational functions work.
Low Temperature Operation	-40°C, 240 hrs	
High Temperature Storage	85°C, 240 hrs	
Low Temperature Storage	-40°C, 240 hrs	
High Temperature/Humidity Operation	60°C, 90% RH, 120 hrs	
Thermal Shock	-40°C $\leftrightarrow$ 85°C, 24 cycles 60 mins dwell	

* The samples used for the above tests do not include polarizer.

* No moisture condensation is observed during tests.

5.2 Failure Check Standard

After the completion of the described reliability test, the samples were left at room temperature for 2 hrs prior to conducting the failure test at $23\pm5^{\circ}\text{C}$; $55\pm15\%$ RH.

6. Outgoing Quality Control Specifications

6.1 Environment Required

Customer's test & measurement are required to be conducted under the following conditions:

Temperature:	$23 \pm 5^{\circ}\text{C}$
Humidity:	$55 \pm 15\% \text{ RH}$
Fluorescent Lamp:	30W
Distance between the Panel & Lamp:	$\geq 50\text{cm}$
Distance between the Panel & Eyes of the Inspector:	$\geq 30\text{cm}$
Finger glove (or finger cover) must be worn by the inspector.	
Inspection table or jig must be anti-electrostatic.	

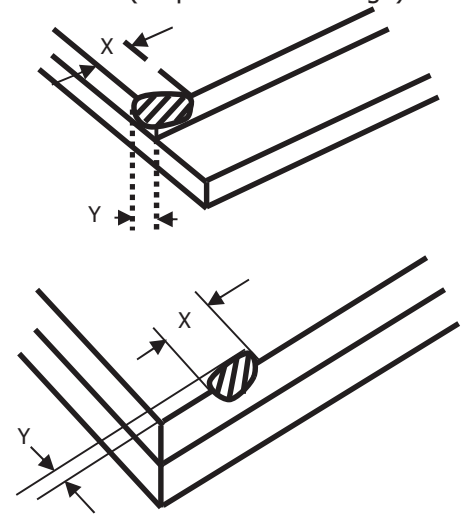
6.2 Sampling Plan

Level II, Normal Inspection, Single Sampling, MIL-STD-105E

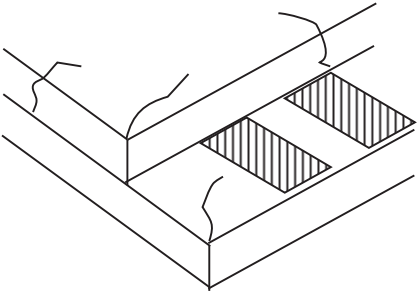
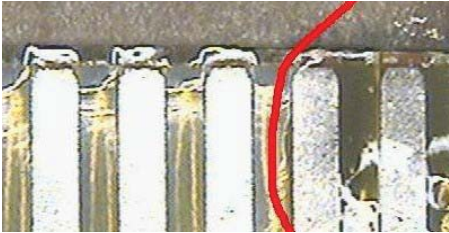
6.3 Criteria & Acceptable Quality Level

Partition	AQL	Definition
Major	0.65	Defects in Pattern Check (Display On)
Minor	1.0	Defects in Cosmetic Check (Display Off)

6.3.1 Cosmetic Check (Display Off) in Non-Active Area

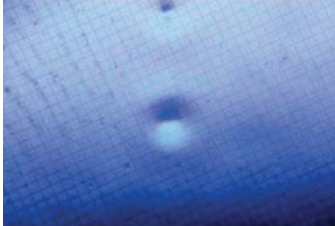
Check Item	Classification	Criteria
Panel General Chipping	Minor	$X > 6 \text{ mm}$ (Along with Edge) $Y > 1 \text{ mm}$ (Perpendicular to edge) 

6.3.1 Cosmetic Check (Display Off) in Non-Active Area (Continued)

Check Item	Classification	Criteria
Panel Crack	Minor	Any crack is not allowable. 
Copper Exposed (Even Pin or Film)	Minor	Not Allowable by Naked Eye Inspection
Film or Trace Damage	Minor	
Terminal Lead Prober Mark	Acceptable	
Glue or Contamination on Pin (Couldn't Be Removed by Alcohol)	Minor	
Ink Marking on Back Side of panel (Exclude on Film)	Acceptable	Ignore for Any

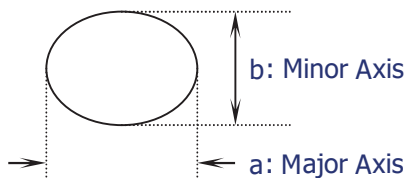
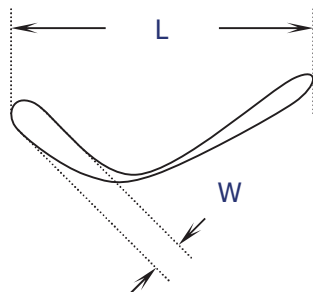
6.3.2 Cosmetic Check (Display Off) in Active Area

It is recommended to execute in clear room environment (class 10k) if actual in necessary.

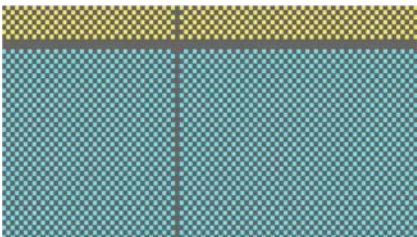
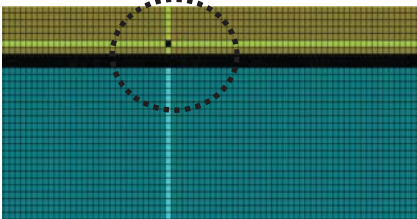
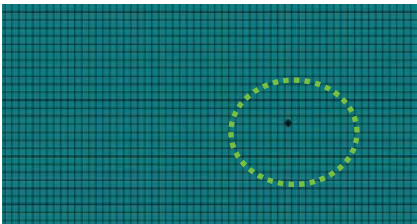
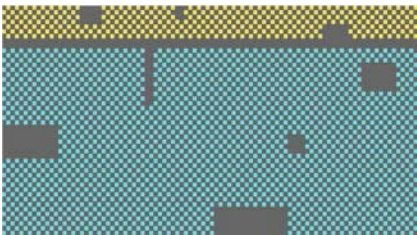
Check Item	Classification	Criteria
Any Dirt & Scratch on Polarizer's Protective Film	Acceptable	Ignore for not Affect the Polarizer
Scratches, Fiber, Line-Shape Defect (On Polarizer)	Minor	$W \leq 0.1$ Ignore $W > 0.1$ $L \leq 2$ $n \leq 1$ $L > 2$ $n = 0$
Dirt, Black Spot, Foreign Material, (On Polarizer)	Minor	$\Phi \leq 0.1$ Ignore $0.1 < \Phi \leq 0.25$ $n \leq 1$ $0.25 < \Phi$ $n = 0$
Dent, Bubbles, White spot (Any Transparent Spot on Polarizer)	Minor	$\Phi \leq 0.5$ → Ignore if no Influence on Display $0.5 < \Phi$ $n = 0$ 
Fingerprint, Flow Mark (On Polarizer)	Minor	Not Allowable

* Protective film should not be tear off when cosmetic check.

** Definition of W & L & Φ (Unit: mm): $\Phi = (a + b) / 2$



6.3.3 Pattern Check (Display On) in Active Area

Check Item	Classification	Criteria
No Display	Major	
Missing Line	Major	
Pixel Short	Major	
Darker Pixel	Major	
Wrong Display	Major	
Un-uniform	Major	