SIEMENS

ICs for Communications

Extended Line Card Interface Controller ELIC®

PEB 20550
PEF 20550

Versions 1.3

User's Manual 01.96

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PEB 20550 PEF 20550 Revision History:		User's Manual 01.96
Previous Release:		Technical Manual 9.93
Page (in Previous Release)	Page (in User's Manual)	Subjects (major changes since last revision)
–	13	PEF 20550 (ext. temperature range; new)
–	38	System Integration and Application (DECT added)
29	46	Boundary scan number 22 = 110 (correction)
29	46	Boundary scan number 9: ID code for V1.3 added
31	49	Boundary scan ID code for V1.3 added
–	57	DMA-transfers, figure 31 (new)
–	60	Support of the HDLC protocol by SACCO, figure 35 (new)
51	76	SACCO clock mode 2 description (extended)
53	80	Extensions for V1.3
55	82	Arbiter state machine description (extended)
58	85	Table 14: Control channel delay examples (extended)
65	95	Internal reference clock RCL replaced by CFI reference clock CRCL
–	101	Interrupt driven transmission sequence example, figure 50 (new)
82	114	Internal reference clock RCL replaced by CFI reference clock CRCL
85	118	Register address arrangement (extended)
–	129	EMOD: ECMD2 restriction 5 (new)
93	130	PMOD: PMD1..0 description (data rate stepping corrected)
101	140	CMD2: CXF, CRR description (corrected)
104	144	MACR description (extended)
114	154	TIMR: SSR (correction)
121	162	VNSR: VN3..0 = V1.2 (correction)
124	167	EXIR: XMR description (extended)
128	172	CCR1: ODS description (extended for V1.3)
132	177	SACCO RSTA: C/R description (new)
140	185	VSTR: VN3..0 value for V1.3 added
142	187	SCV: SCV7...0 description (extended)
–	191	Application Hints (new)
148	380	$t_{ALD\,min}$ = 8 ns, $t_{DRH\,max}$ = 65 ns, $t_{AH\,min}$ = 0 ns (correction)
–	395	Package outlines (new)
–	396	Appendix (new)

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1 Overview

The PEB 20550 (**E**xtended **L**ine Card **C**ontroller) is a highly integrated controller circuit optimized for line card and key system applications. It combines all functional blocks necessary to manage up to 32 digital (ISDN or proprietary) or 64 analog subscribers.

The switching and layer-1 control capability of the EPIC-1 (PEB 2055) constitutes a major functional block of the ELIC.

For layer-2 support, two independent Special Application Communication Controllers (SACCO) are available. One typically handles the communication with the group controller, the other is used to serve the subscriber terminals. A D-channel arbiter is employed to multiplex the HDLC controller between multiple subscribers while maintaining full duplex signaling protocols (e.g. LAPD).

Additionally, typical line card glue logic functions such as a power-up reset generator, a watchdog timer and two parallel ports are integrated.

The ELIC is implemented in a Siemens advanced 1.0-µm CMOS-technology and manufactured in a P-MQFP-80-1 package.

The ELIC is a member of a new chip family supporting D-channel multiplexing on the line card and in the subscriber terminal. This concept allows an highly economical implementation of digital subscriber lines.

Chip Family

Line Cards:

PEB 20550	Extended Line Card Controller	(ELIC)
PEB 2096	Octal U_{PN} Transceiver	(OCTAT-P)
PEB 2095	ISDN Burst Transceiver Circuit	(IBC)
PEB 2084	QUAD S_0 Transceiver	(QUAT-S)
PEB 2465	QUAD DSP based Codec Filter	(SICOFI-4)
PEB 2075	ISDN D-Channel Exchange Controller	(IDEC)

Terminals:

PSB 2196	Digital Subscriber Access Controller for U_{PN} Interface	(ISAC-P TE)
PEB 2081 (V3.2)	S/T-Bus Interface Circuit Extended	(SBCX)

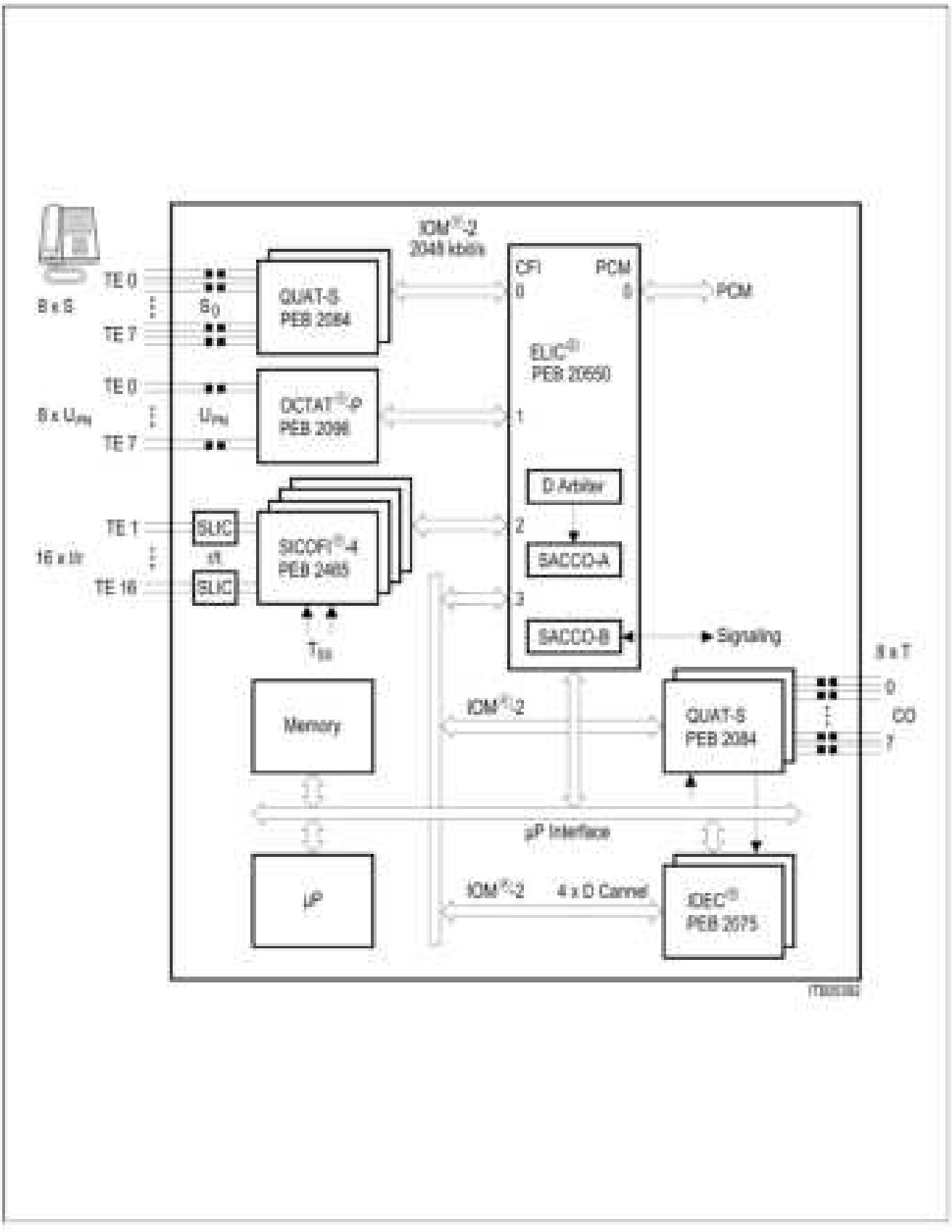

Figure 1
Example for an Integrated Analog / Digital PBX

SIEMENS

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CMOS

1.1 Features

P-MQFP-80-1

Switching (EPIC®-1)

- Non-blocking switch for 32 digital (e.g. ISDN) or 64 voice subscribers
  - Bandwidth 16, 32, or 64 kbit/s
  - Two consecutive 64-bit/s channels can be switched as a single 128-kbit/s channel
- Freely programmable time slot assignment for all subscribers
- Synchronous µP-access to two selected channels
- Two types of serial interfaces independently programmable over a wide data range (128 - 8192 kbit/s)
  - PCM-interface
    Tristate control signals for external drivers
    Programmable clock shift
    Single or double data clock
  - Configurable interface
    Configurable for IOM-, SLD- and PCM-applications
    High degree of flexibility for datastream adaption
    Programmable clockshift
    Single or double data clock

Type	Ordering Code	Package
PEB 20550	Q67101-H6484	P-MQFP-80-1 (SMD)
PEF 20550	Q67101-H6605	P-MQFP-80-1 (SMD)

Handling of Layer-1 Functions (EPIC®-1)

- Change detection for C/I-channel (IOM-configuration) or feature control (SLD-configuration)
- Additional last-look logic for feature control (SLD-configuration)
- Buffered monitor (IOM-configuration) or signaling channel (SLD-configuration)

Handling of Layer-2 Functions (SACCO)

- Two independent full duplex HDLC-channels
  - Serial interface
    Data rate up to 4 Mbit/s
    Independent time slot assignment for each channel with programmable time slot length (1-256 bits)
    Support of bus configuration with collision resolution
    Continuous transmission of 1 to 32 bytes possible
  - Protocol support
    Auto-mode, fully compatible to PEB 2050 (PBC) protocol
    Non-auto mode, address recognition capability
    Transparent mode, HDLC-framing only
    Extended transparent mode, fully transparent without HDLC-framing
  - 64-bytes FIFO's per HDLC-channel and direction

D-channel Multiplexing (D-channel arbiter)

- Serving of multiple subscribers with one HDLC-controller
- Full duplex signaling protocols (e.g. LAPD or proprietary) supported
- Programmable priority scheme
- Broadcast transmission

Line Card Glue Logic

- Power-up reset generator
- Watchdog timer
- Parallel ports (8-bit input, 4-bit I/O)

Boundary Scan Support

- Fully IEEE 1149.1 compatible
- 32-bit device identification register

Bus Interface

- Siemens/Intel or Motorola type µP-interface
- 8-bit demultiplexed bus interface
- FIFO-access interrupt or DMA controlled

1.2 Pin Configuration
(top view)

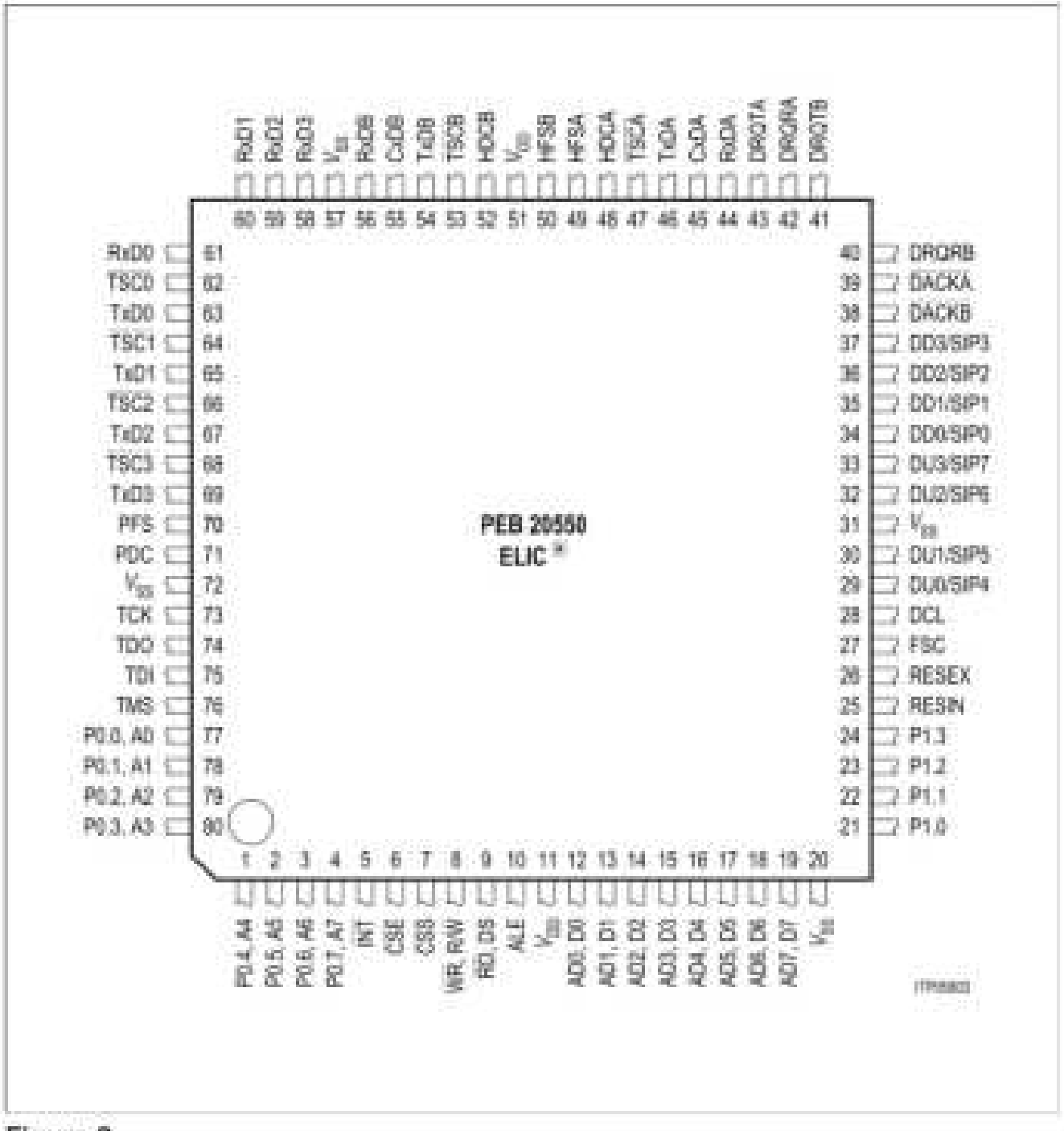

Figure 2