

PRODUCT SPECIFICATION

TFT LCD MODULE

MODEL : SPEC-KWH050ST26-S01 Version: 1.0

【 】 Preliminary Specification

【 ◆ 】 Finally Specification

CUSTOMER'S APPROVAL Chunho Tech	
SIGNATURE:	DATE:

- It signifies that you fully understand and accept all the contents of this specification if you sign and send back the first page of this specifications.

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- This specification is subject to change without notice. Please contact FORMIKE or it's representative before designing your product based on this specification.

Revision record

[illegible]

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1. General Description

1.1 Description

KWH050ST26-S01 is a Transmissive type color active matrix liquid crystal display (LCD), which uses amorphous thin film transistor (TFT) as switching devices. This product is composed of a TFT LCD panel, driver IC, FPC,CTP and backlight unit . The following table described the features of FORMIKE KWH050ST26-S01.

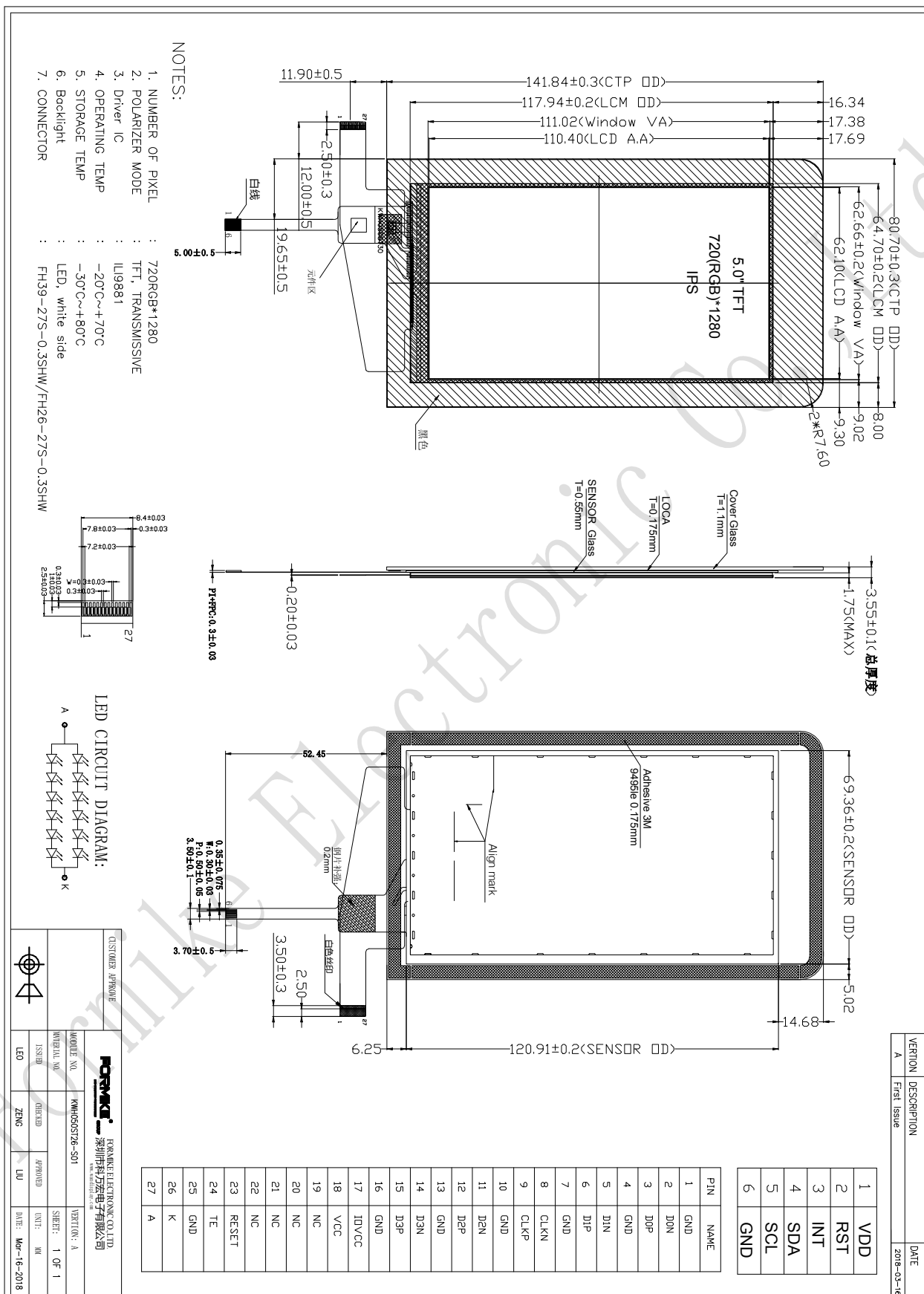
1.2 Application

Mobile phone, Multimedia products
and other electronic Products
Etc.

1.3 Features:

Features	Description	UNITS
LCD type	5.0" TFT	--
Dot arrangement	720 (RGB) × 1280	dots
Driver IC	ILI9881	--
Color Depth	16M	
Interface	4 LANES MIPI	
Module size	80.70(W) × 141.84 (H) × 3.55(T)	mm
Active area	62.10(W) × 110.40(H)	mm
Dot pitch	0.08625 (W) × 0.08625 (H)	mm
Back Light	12 White LED	--
With/Without TSP	With TSP	
Weight(g)	TBD	

2. External Dimensions



3. Interface Description

PIN NO.	PIN NAME	DESCRIPTION
1	GND	Ground.
2	D0N	MIPI DSI differential data pair. (Data lane 0)
3	D0P	MIPI DSI differential data pair. (Data lane 0)
4	GND	Ground.
5	D1N	MIPI DSI differential data pair. (Data lane 1)
6	D1P	MIPI DSI differential data pair. (Data lane 1)
7	GND	Ground.
8	CLKN	MIPI DSI differential clock pair
9	CLKP	MIPI DSI differential clock pair
10	GND	Ground.
11	D2N	MIPI DSI differential data pair. (Data lane 2)
12	D2P	MIPI DSI differential data pair. (Data lane 2)
13	GND	Ground.
14	D3N	MIPI DSI differential data pair. (Data lane 3)
15	D3P	MIPI DSI differential data pair. (Data lane 3)
16	GND	Ground.
17	IOVCC	Power supply for internal logic regulator.
18	VCC	Power supply for analog circuits.
19	NC(SCL)	Serial Clock in the SPI interface, Fix VSS when not in use.
20	NC(SDI)	Serial data input pin for SPI Interface.Leave it open when not in use.
21	NC(CS)	chip select signal for SPI Interface.Fix to VSS when not in use.
22	NC(D/C)	command or parameter select for SPI Interface.Fix to VSS when not in use.
23	RESET	System reset pin
24	TE	Tearing effect output pin.Leave it open when not in use.
25	GND	Ground.
26	K	Cathode input for backlight
27	A	Anode input for backlight

4. Absolute Maximum Ratings

The absolute maximum rating is listed in Table 36. When the IL19881 is used out of the absolute maximum ratings, it may be permanently damaged. To use the IL19881 within the following electrical characteristics limit is strongly recommended for normal operation. If these electrical characteristic conditions are exceeded during normal operation, the IL19881 will malfunction and cause poor reliability.

Table 36: Absolute Maximum Ratings

Item	Symbol	Unit	Value
Analog Operating Voltage	VCI - GND	V	-0.3 ~ +5.5
Analog Operating Voltage	VOREF - GND	V	-0.3 ~ +5.5
Digital Operating Voltage	VDDI - GND	V	-0.3 ~ +3.3
DSI Operating Voltage	VDDAM - GND	V	-0.3 ~ +3.3
OTP Supply Voltage	MTP_PWR - GND	V	-0.3 ~ +8.0
Supply Voltage	VSP - GND	V	-0.3 ~ +6.0
Supply Voltage	VBN - GND	V	0.3 ~ -8.0
Gate Driver High Voltage	VGH - GND	V	-0.3 ~ +18
Gate Driver Low Voltage	VGL - GND	V	0.3 ~ -18
Driver Supply Voltage	VCI - VOL	V	≤ 6.0V
Driver Supply Voltage	VGH - VGL	V	≤ 32.0V
Input Voltage	VIN	V	-0.3 ~ VDDI + 0.3
HS Input Voltage	VHSIN	V	-0.3 ~ + 1.65
Operating Temperature	T _{opr}	°C	-50 ~ +75
Storage Temperature	T _{stg}	°C	-55 ~ +110

Note: Even if the absolute maximum rating of one of the above parameters is exceeded only for a short while, the quality of the product may be degraded. Therefore, be sure to use the product within the range of the absolute maximum ratings.

5. Electrical Characteristics

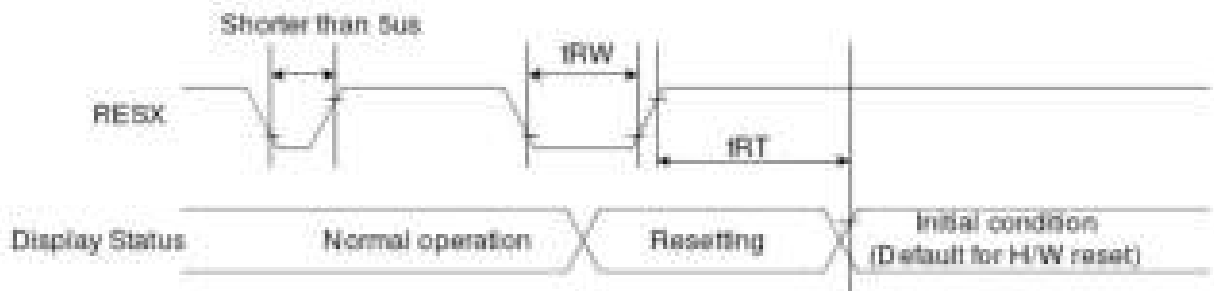
Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Power & Operation Voltage							
Analog operating voltage	VCI	-	2.5	2.8	3.3	V	Note1
Analog operating voltage	VCIREF	-	2.5	2.8	3.3	V	Note1
Digital operating voltage	VDDI	-	1.65	2.8	3.3	V	Note1
DGI operating voltage	VDDAM	-	1.65	1.8	3.3	V	Note1
OTP Supply voltage	MTF_PWR	-	7.25	7.5	7.75	V	Note1
Logic High level input voltage	V _{IH}	-	0.7*VDDI		VDDI	V	Note1
Logic Low level input voltage	V _{IL}	-	-0.3		0.2*VDDI	V	Note1
Logic High level output voltage TE, TE1, SDI, LEOPWM	V _{OH}	I _{OH} = -1.0mA	0.9*VDDI		VDDI	V	Note1
Logic Low level output voltage TE, TE1, SDI, LEOPWM	V _{OL}	I _{OL} = +1.0mA	0		0.2*VDDI	V	Note1
Gate Driver High Voltage	V _{GH}	-	8.5	-	18	V	
Gate Driver Low Voltage	V _{GL}	-	-15.0	-	-7.5	V	
Driver Supply Voltage	-	(V _{GH} -V _{GL})	15	-	30	V	
VCOM Operation							
DC VCOM Amplitude Voltage	VCOM	-	-4.3	-	0	V	Note3
Source Driver							
Source Output Range	V _{SOUT}	-	0.5	-	V _{REG1OUT} -3.5	V	Note4
Positive Gamma Reference Voltage	V _{REG1OUT}	-	2.8	-	3.5	V	
Negative Gamma Reference Voltage	V _{REG2OUT}	-	-5.5	-	-2.8	V	
Source Output Setting Time	T _r	Source with 50% precision	-	10 (TBD)	-	μs	Note3,4
Output Deviation Voltage (Source Output channel)	V _{error}	Source=4.2V Source=0.5V	-	-	30 (TBD)	mV	Note3
		4.2V>Source>0.5V	-	-	15 (TBD)	mV	
Output Offset Voltage	V _{OFFSET}	-	-	-	35 (TBD)	mV	Note3
Booster Operation							
Booster (VCIx2) Voltage	V _{SP}	-			5	V	
Booster (VCIx3) Voltage	V _{SN}	-	-8			V	
Standby mode current consumption							
Sleep to mode	(VDDI SLP IN)	T _a = 25 °C VCI=2.8V VDDI=1.3V	-	(TBD)	(TBD)	μA	
	(VCI SLP IN)		-	(TBD)	(TBD)	μA	
Deep Standby mode	(VDDI DSTR)		-	1	-	μA	
	(VCI DSTR)		-	1	-	μA	

Notes:

1. T_a = -30 to 70 °C (to 85 °C no damage) , VCI = VCIREF = 2.5V to 3.3V, VDDI = VDDAM = 1.65V to 3.3V
2. Supply digital VDDI voltage equal or less than analog VCI voltage
3. Source channel loading = (TBD)
4. The maximum value is between with (TBD) and Gamma setting value

6.Timing Characteristics.

6.1 Reset Timing Characteristics.



Signal	Symbol	Parameter	Min	Max	Unit
RESX	tRW	Reset pulse duration	10		uS
	tRT	Reset cancel		5 (note 1,5)	mS
				120 (note 1,6,7)	mS

Note 1: The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NV memory to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.

Note 2: Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 10us	Reset
Between 5us and 10us	Reset starts

Note 3: During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In -mode.) And then return to Default condition for Hardware Reset.

Note 4: Spike Rejection also applies during a valid reset pulse as shown below:



Note 5: When Reset applied during Sleep In Mode.

Note 6: When Reset applied during Sleep Out Mode.

Note 7: It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

6.2 Interface Timing Characteristics.

6.2.1 High Speed Mode-Clock Channel Timing.

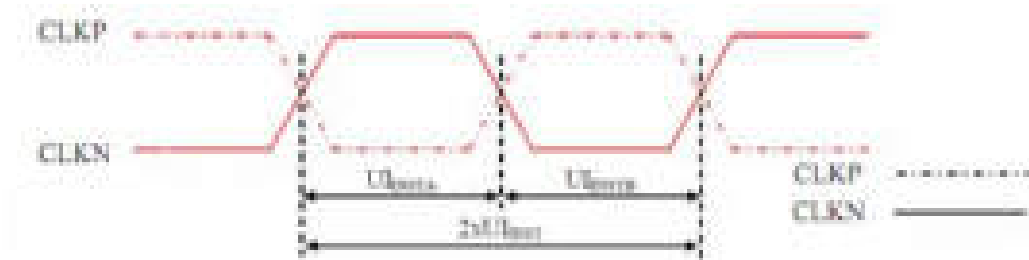


Figure: DSI Clock Channel Timing

Table: DSI Clock Channel Timing

Signal	Symbol	Parameter	Min	Max	Unit
CLKPn	$2xUI_{inst}$	Double UI instantaneous	4	25	ns
CLKPn	UI_{inst}, UI_{inst} (Note 1)	UI instantaneous Half	2 (Note 2)	12.5	ns

Notes:

1. $UI = UI_{INSTA} + UI_{INSTB}$
2. Define the minimum value of 24 UI per Pixel, see Table.

Table: Limited Clock Channel Speed

Data type	Two Lanes speed	Three Lanes speed	Four Lanes speed
Data Type = 00 1110 (2Bn), RGB 555, 18 UI per Pixel	555 Mbps	433 Mbps	360 Mbps
Data Type = 01 1110 (3Bn), RGB 555, 18 UI per Pixel	637 Mbps	487 Mbps	412 Mbps
Data Type = 10 1110 (2Bn), RGB 555 Loosely, 24 UI per Pixel	650 Mbps	650 Mbps	650 Mbps
Data Type = 11 1110 (3Bn), RGB 555, 24 UI per Pixel	650 Mbps	650 Mbps	650 Mbps

6.2.2 High Speed Mode-Data Clock Channel Timing .

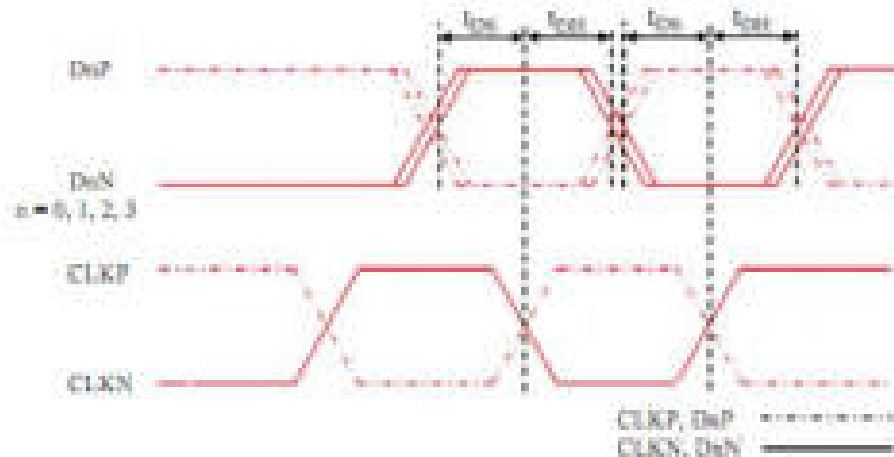


Figure: DSI Data to Clock Channel Timings

Table: DSI Data to Clock Channel Timings

Signal	Symbol	Parameter	Min	Max
DnPN, n=0 and 1	t_{sa}	Data to Clock Setup time	0.15ns	-
	t_{sh}	Clock to Data Hold Time	0.15ns	-

6.2.2 High Speed Mode-Rising and Falling Timings .

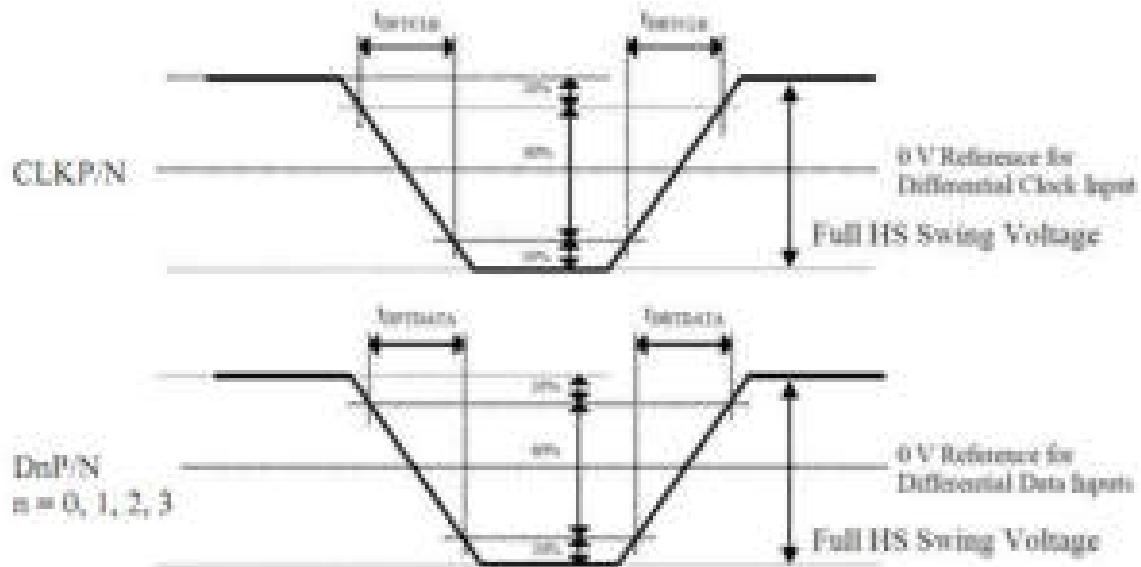


Figure: Rising and Falling Timings on Clock and Data Channels

Table: Rise and Fall Timings on Clock and Data Channels

Parameter	Symbol	Condition	Specification		
			Min.	Typ.	Max.
Differential Rise Time for Clock	$t_{riseCLK}$	CLKP/N	150 ps	-	0.3UI (Note)
Differential Rise Time for Data	$t_{riseDATA}$	DnPIN (n=0 and 1)	150 ps	-	0.3UI (Note)
Differential Fall Time for Clock	$t_{fallCLK}$	CLKP/N	150 ps	-	0.3UI (Note)
Differential Fall Time for Data	$t_{fallDATA}$	DnPIN (n=0 and 1)	150 ps	-	0.3UI (Note)

Note: The display module has to meet timing requirements, which are defined for the transmitter (MCU) on MIPI D-Phy standard.

6.2.3 Low Speed Mode-Bus Turn Around.

Lower Power Mode and its State Periods on the Bus Turnaround (BTA) from the MCU to the Display Module (LI9881) are illustrated for reference purposes below.

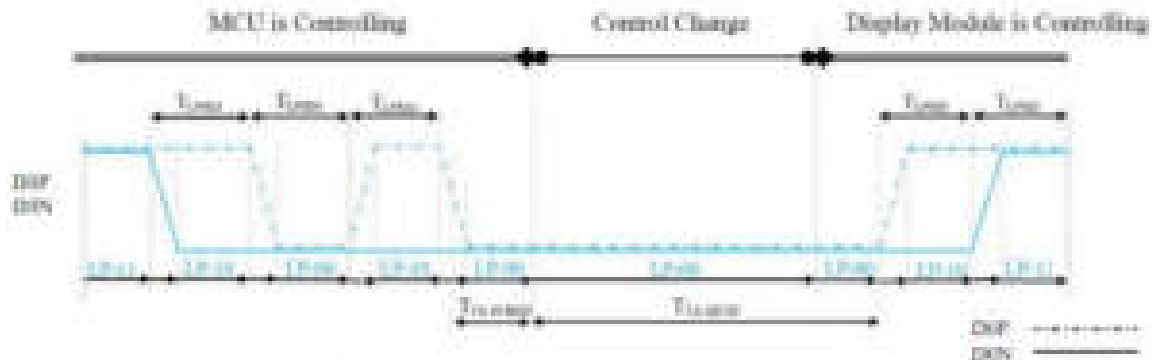


Figure: BTA from the MCU to the Display Module

Lower Power Mode and its State Periods on the Bus Turnaround (BTA) from the Display Module (LI9881) to the MCU are illustrated for reference purposes below.

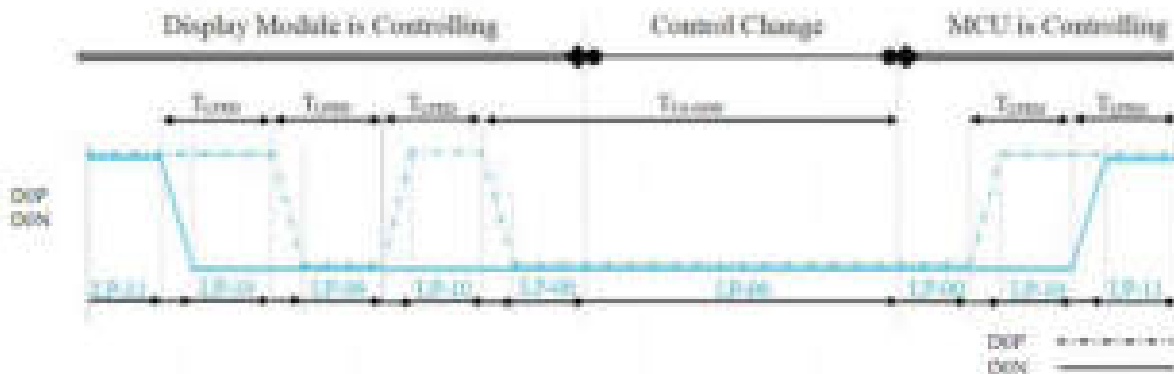


Figure: BTA from the Display Module to the MCU

Table: Low Power State Period Timings – A

Signal	Symbol	Description	Min	Max	Unit
D0P/N	T_{LP-00}	Length of LP-00, LP-01, LP-10 or LP-11 periods MCU → Display Module (LI9881)	50	75	ns
D0P/N	T_{LP-01}	Length of LP-00, LP-01, LP-10 or LP-11 periods Display Module (LI9881) → MCU	50	75	ns
D0P/N	$T_{LP-00+01}$	Time-out before the Display Module (LI9881) starts driving	T_{LP-00}	$2 \times T_{LP-00}$	ns

Table: Low Power State Period Timings – B

Signal	Symbol	Description	Time	Unit
D0P/N	T_{LP-00}	Time to drive LP-00 by Display Module (LI9881)	$5 \times T_{LP-00}$	ns
D0P/N	T_{LP-00}	Time to drive LP-00 after turnaround request - MCU	$4 \times T_{LP-00}$	ns

6.2.6 DSI Clock Burst-High Speed Mode to/from Low Power Mode .

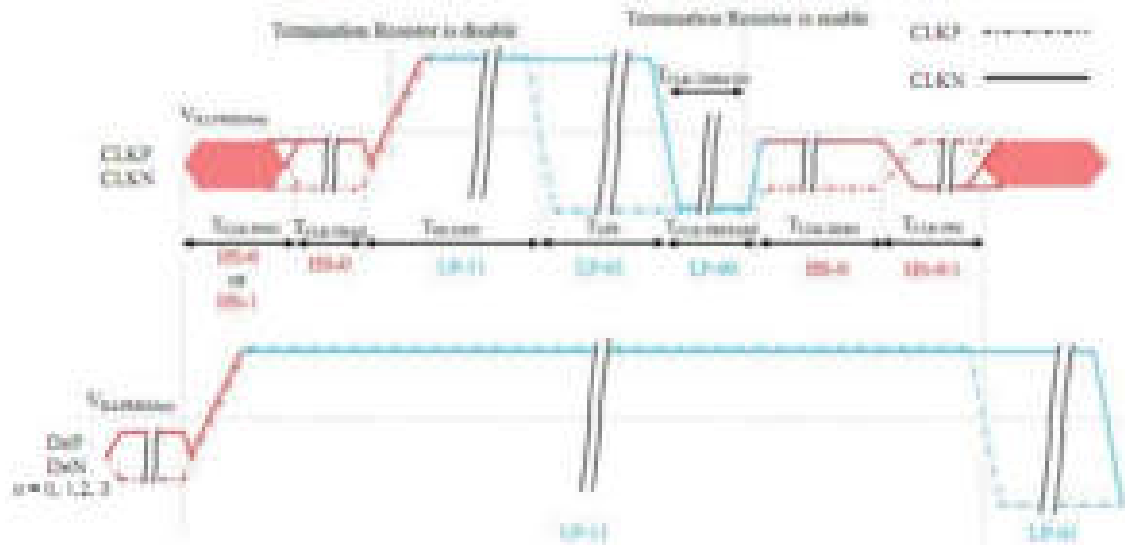
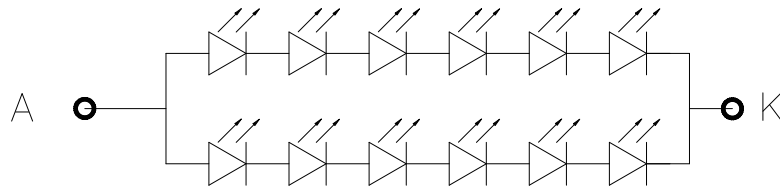


Figure 124: Clock Lanes - High Speed Mode to/from Low Power Mode Timings

Table 46: Clock Lanes - High Speed Mode to/from Low Power Mode Timings

Signal	Symbol	Description	Min	Max	Unit
CLRP/N	T_{clkp6}	Time that the MCU shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode	50-52xUI	-	ns
CLRP/N	T_{clkp7}	Time to drive HS differential state after last payload clock bit of a HS transmission burst	50	-	ns
CLRP/N	T_{clkp1}	Time to drive LP-11 after HS burst	100	-	ns
CLRP/N	T_{clkp2}	Time to drive LP-00 to prepare for HS transmission	38	95	ns
CLRP/N	T_{clkp3}	Time-out at Clock Lane to enable HS termination	-	38	ns
CLRP/N	$T_{clkp4} + T_{clkp5}$	Minimum HS-0 drive period before starting Clock	300	-	ns
CLRP/N	T_{clkp5}	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	5xUI	-	ns

7. Backlight Characteristics.



Item	Symbol	MIN	TYP	MAX	UNIT	Test Condition	Note
Supply Voltage	V_f	18.0	19.2	20.4	V	I_f=40 mA	-
Supply Current	I_f	-	40	-	mA	-	-
Reverse Voltage	V_r	-	-	5	V	10uA	
Power dissipation	P_d	-	768	-	mW	-	
Luminous Intensity for LCM		180	200	220	Cd/m²	I_f=40 mA	
Uniformity for LCM	-	80	-	-	%	I_f=40 mA	
Life Time	-	50000	-	-	Hr	I_f=40 mA	-
Backlight Color	White						

8. Touch panel Characteristics.

8.1 Interface Description:

PIN NO.	PIN NAME	DESCRIPTION
1	VDD	Power supply voltage
2	RST	Reset for system
3	INT	Interrupt output for CTP.
4	SDA	Data signal for IIC interface.
5	SCL	Clock signal for IIC interface.
6	GND	Ground

8.2 Features :

Item	Description
Interface	IIC
Touch Linearity	3%
Surface hardness	≥6H
Transmittance	≥85%
Structure type	G+G(Glass+Glass)
Lifetime	≥1,000,000 times
Driver IC	FT5216
Touch points	5 fingers

8.3 Electronic Characteristics :

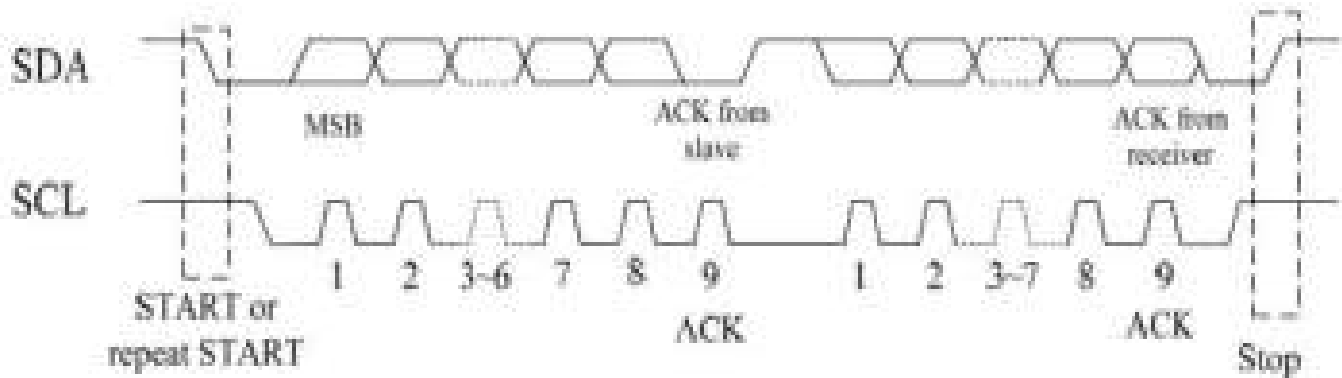
Item	Symbol	MIN	TYP	MAX	UNIT	Test Condition	Note
Supply Voltage	VCC	2.8	3.3	3.6	V		-
Input high-level voltage	VIH	0.7*VCC	-	VCC	V		
Input low -level voltage	VIL	-0.3		0.3*VCC	V		
Output high -level voltage	VOH	0.7*VCC	-	-	V		
Output low -level voltage	VOL	-	-	0.3*VCC	V		

8.4 IIC Interface Timing.

IIC Timing Characteristics.

Parameter	Unit	Min	Max
SCL frequency	KHz	0	400
Bus free time between a STOP and START condition	us	4.7	∞
Hold time (repeated) START condition	us	4.0	∞
Data setup time	us	250	∞
Setup time for a repeated START condition	us	4.7	∞
Setup Time for STOP condition	us	4.0	∞

I2C Serial Data Transfer Format.



I2C master read, slave write.

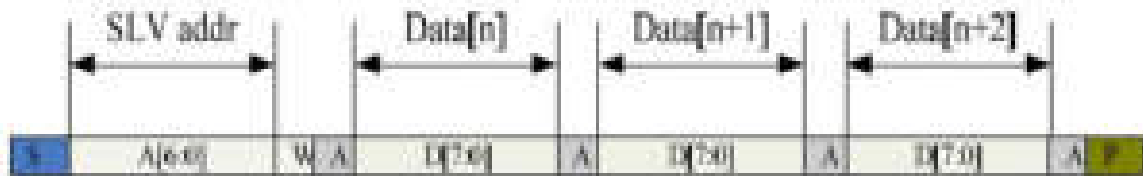
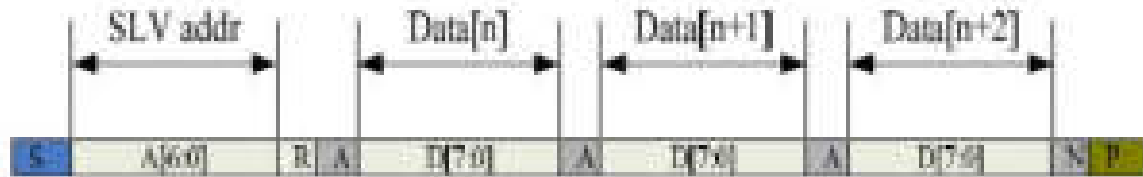


Figure 2-5 I2C master write, slave read



Mnemonics Description.

Mnemonics	Description
S	I2C Start or I2C Restart
A[6:0]	Slave address A[6:0]: address bits are identical to those of I2C.ADDR [7:1] register
R/W	'1' for read, '0' for write
A(N)	ACK(NACK)
P	STOP: the indication of the end of a packet (if this bit is missing, S will indicate the end of the current packet and the beginning of the next packet)

9.Optical Characteristics

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Transmittance (with Polarizer)		T (%)	$\Theta=0$ Normal viewing angle	—	3.3	—	%	Measuring with Polarizer - Reference Only
Transmittance (without Polarizer)		T (%)		—	10.7	—	%	
Contrast		CR		640	800	—	—	(1)(2)
Response time	Rising	T _R		—	10	15	msec	(1)(3)
	Falling	T _F		—	20	25		
Color gamut	(%)			—	70	—	%	C-light
Color chromaticity (CIE1931)	White	W _x		Normal viewing angle	(0.283)	(0.303)	(0.323)	—
		W _y	(0.303)		(0.323)	(0.343)		
	Red	R _x	(0.634)		(0.654)	(0.674)	—	
		R _y	(0.299)		(0.319)	(0.339)	—	
	Green	G _x	(0.239)		(0.259)	(0.279)	—	
		G _y	(0.554)		(0.574)	(0.594)		
	Blue	B _x	(0.120)		(0.140)	(0.160)	—	
		B _y	(0.064)		(0.084)	(0.104)		
Viewing angle	Hor.	Θ_L	CR>10	—	80	—	—	(1)(4) Measuring with Polarizer - Reference Only
		Θ_R		—	80	—		
	Ver.	Θ_U		—	80	—		
		Θ_D		—	80	—		
Optima View Direction		Free						(5)

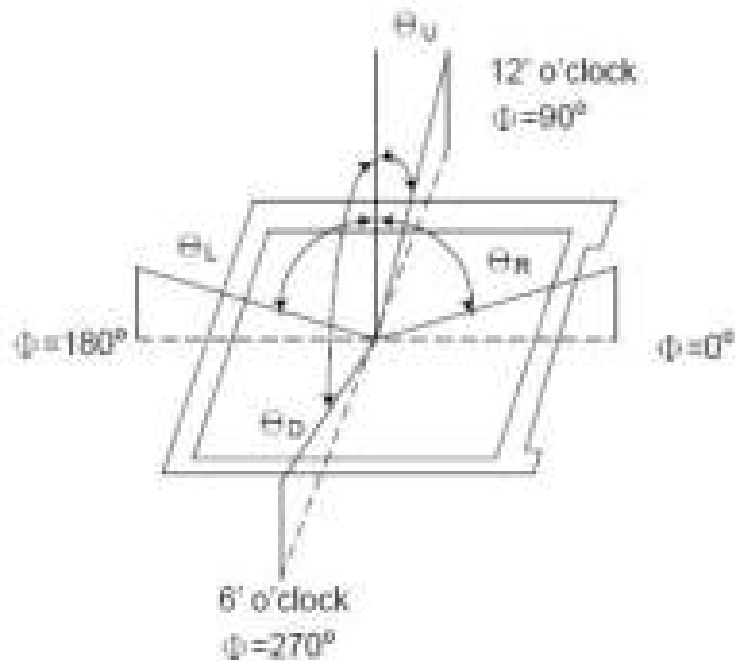
Measuring Condition

- Measuring surrounding : dark room
- Ambient temperature : $25\pm2^{\circ}\text{C}$
- 15min. warm-up time.

Measuring Equipment

- FPM520 of Westar Display technologies, INC., which utilized SR-3 for Chromaticity and BM-5A for other optical characteristics.

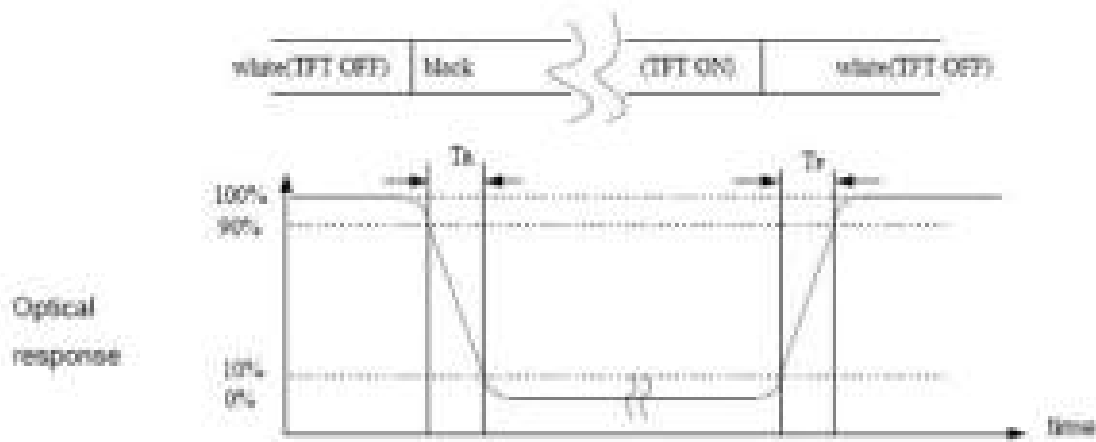
Note (1) Definition of Viewing Angle :



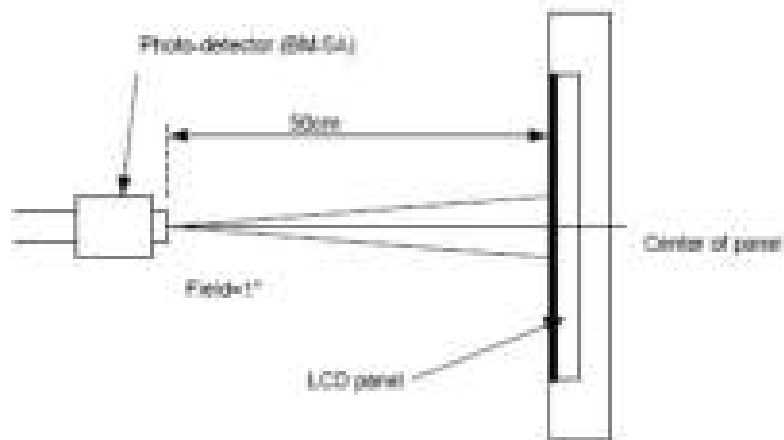
Note (2) Definition of Contrast Ratio(CR) :
measured at the center point of panel

$$CR = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

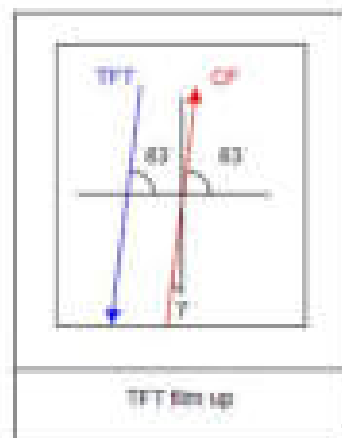
Note (3) Definition of Response Time : Sum of T_R and T_F



Note (4) Definition of optical measurement setup



Note (5) Rubbing Direction (The different Rubbing Direction will cause the different optima view direction.)



10. RELIABILITY

No.	Test Item	Test Condition	Remark
1	High Temperature Storage	+80℃± 2℃, 96 hrs	Note
2	Low Temperature Storage	-30℃± 2℃, 96 hrs	Note
3	High Temperature Operation	+70℃± 2℃, 96 hrs	Note
4	Low Temperature Operation	+20℃± 2℃, 96 hrs	Note
5	High Temperature & High Humidity Storage Test	+50℃± 5℃, 90%R.H, 96 hours	Note
6	Temperature Cycle (non operation)	-30℃ ← +25℃ → +80℃ (30mins ← 5mins → 30mins) 10 Cycles	Note
7	Electronic Static Discharge	Air Discharge: 2KV to with 5 times	Discharge for each polarity Mode of Operation: Single Discharge, successive discharge at least 1 sec
		Ambiance: 15℃~35℃, 30%~60%R.H Resistance(Rd): 330Ω ±10% Capacitance(Cs + Cd): 150pF±10%	
8	Vibration (Packaged)	Frequency range: 10Hz ~ 55 Hz Amplitude: 1.5mm Direction of X.Y. Z for 3 Hrs in total	
9	Drop Test (Packaged)	Height: 80cm, Time: 1 1 corner, 3 edged, 6 surfaces	

Note : Recovery Time should be 2~4 hours at room temperature (20±8℃) and humidity (below 60% R.H). No abnormalities in functions and appearance

11.INSPECTION CRITERION

11.1 Scope

Display Quality Evaluation

Mechanics Specification

11.2 Sampling Plan

MIL-STD-105E

Unless there is other agreement, the sampling plan for incoming inspection shall follow MIL-STD-105E

Lot size: Quantity per shipment as one lot (different model as different lot).

Sampling type: Normal inspection, single sampling

Sampling level: Level II.

11.3 Acceptable Quality Level

Item	Major	Minor
Appearance	1.0%	1.5%
Electrical	0.65	1.0%

11.3.1 Classification of defects:

11.3.1.1Major defect

Any defect may result in functional failure, or reduce the usability of product for its purpose. For

Example: Electrical failure, deformation and etc.

11.3.1.2 Minor defect

The criteria on major or minor judgment will be according with the classification of defects.

11.4 Panel Inspection Condition

11.4.1 Environment:

11.4.2 Room Temperature: $25 \pm 5^{\circ}$ C.

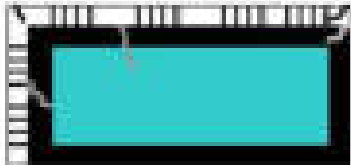
11.4.3 Humidity: $50 \pm 20\%$ RH.

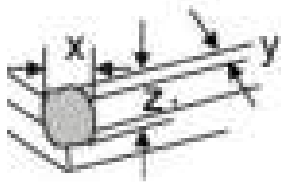
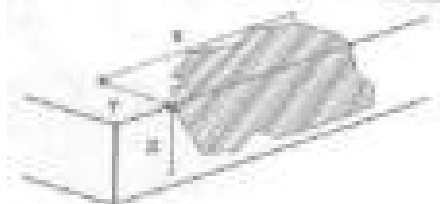
Illumination: 300 ~ 700 Lux.

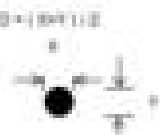
11.4.4 Inspection Distance: 35 ± 5 cm

11.5 TFT Inspection Criteria

11.5.1 Visual inspection criterion in cosmetic / appearance

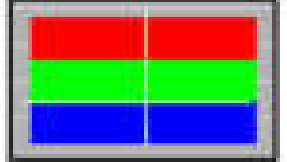
Glass defect			
N o	Item	Criteria	Remark
1	Dimension (Minor)	By engineering diagram	
2	Crack (Major)	Extensive crack	

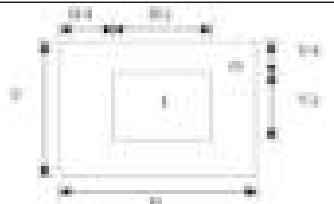
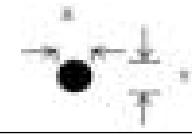
3	Corner (Minor)	$X \leq 3 \text{ mm}$ $Y \leq 3 \text{ mm}$ $Z \leq T$ Ignore	 T: Glass thickness Z: Thickness X: Length Y: Width
4	Side (Minor)	$X \leq 5 \text{ mm}$ $Y \leq 3 \text{ mm}$ $Z \leq T$ Ignore	 T: Glass thickness Z: Thickness X: Length Y: Width

TFT defect in appearance			
No	Item	Criteria	Remark
1	Foreign Spot (Minor) Including: Black spot, White spot Pin hole Foreign particle	$D \leq 0.25 \text{ mm}$, Ignore $0.25 \text{ mm} < D \leq 0.5 \text{ mm}$, $N \leq 3$ $0.5 \text{ mm} < D$, $N = 0$ Distance $\geq 5 \text{ mm}$ Ignore if out of Area AA	$D = (X+Y)/2$, X: Length, Y: Width 
2	Foreign Line(Minor) Including: Black line White line Bright line	$W \leq 0.03 \text{ mm}$, Ignore $0.05 \text{ mm} < W \leq 0.08 \text{ mm}$, $L \leq 4 \text{ mm}$, $N \leq 3$ $0.08 \text{ mm} < W \leq 0.10 \text{ mm}$, $L \leq 4 \text{ mm}$, $N \leq 1$ $W > 0.10 \text{ mm}$, $N = 0$ Ignore if out of Area AA	L: Length, W: Width 
3	Polarizer Dent/Air Bubble (Minor)	$D \leq 0.25 \text{ mm}$, Ignore $0.25 \text{ mm} < D \leq 0.5 \text{ mm}$, $N \leq 4$ $D > 0.50 \text{ mm}$, $N = 0$ Distance $\geq 5 \text{ mm}$	$D = (X+Y)/2$, X: Length, Y: Width 
4	Polarizer Scratches (Minor)	$W \leq 0.05 \text{ mm}$, Ignore $0.05 \text{ mm} < W \leq 0.08 \text{ mm}$, $L \leq 4 \text{ mm}$, $N \leq 3$ $0.08 \text{ mm} < W \leq 0.10 \text{ mm}$, $L \leq 4 \text{ mm}$, $N \leq 1$ $W > 0.10 \text{ mm}$, $N = 0$ Ignore if out of Area AA	L: Length, W: Width 

Other defects			
No	Item	Criteria	Remark
1	FPC (Minor)	Any crack or breakage which effect the function are not allowed Disregard if the dirty removed	
2	Backlight (Minor)	Power up is allowed. Breaking off is not allowed. The scratch which may causes a problem in practical use is not allowed	
3	Bezel (Minor)	Erasable dirt is ignore	

11.5.2 Visual inspection criterion in electrical display

Glass defect			
No	Item	Criteria	Remark
1	No display (Major) Abnormally Short circuit	Not allowed	
2	Missing line (Major)	Not allowed	
3	Darker or lighter line (Major)	Not allowed	
4	Weak line (Minor)	By limit sample	

Display Inspection						
No	Item	Criteria				Remark
1	Bright / Dark dot	Items	Area I	Area O	Tota I	 1.1sub-pixel: 1R or 1G or 1B 2.Point defect area ≥ 1/2 sub pixel
		Bright	1	2	2	
		Dark	2	3	4	
		Bright & Dark	2	4	5	
		2 adjacent dots	0	0	0	
		Minimum Distance ≥ 5mm				
2	Tiny bright dot	Visible through 6% ND filter D≤0.25mm, Ignore 0.25mm<D≤0.5mm, N≤4 D>0.5mm, N=0 Distance≥5mm Ignore if out of Area AA				D =(X+Y)/2, X: Length, Y: Width 
4	Mura/Waving/ Hot spot	Not visible through 6% ND filter in 50% gray or judge by limit sample if necessary				

* Note:

- Defect which is on the Black Matrix (outside of active area) are not considered as a defect.
- If any specific defect is not included in the above defect table, this defect should be judged by Formike.
- W: Width, L: Length D: Average Diameter N: Count.

12. PRECAUTION RELATING & PRODUCT HANDLING

Display is assembled and adjusted with a high degree of precision. Do not attempt to make any alteration or modification.

12.1 SAFETY

12.1.1 If the LCD panel breaks, be careful not to get the liquid crystal to touch your skin.

12.1.2 If the liquid crystal touches your skin or clothes, please wash it off immediately by using soap and water.

12.2 HANDLING

12.2.1 Avoid any strong mechanical shock which can break the glass.

12.2.2 Avoid static electricity which can damage the CMOS LSI - When working with the module, be sure to ground your body and any electrical equipment you may be using. The followings should be noted:

12.2.2.1 CMOS-LSI is used for the module circuit; therefore operators should be grounded whenever he/she comes into contact with the module.

12.2.2.2 Do not touch any of the conductive parts such as the LSI pads; the copper leads on the PCB and the interface terminals with any parts of the human body.

12.2.2.3 Do not touch the connection terminals of the display with bare hand; it will cause disconnection or defective insulation of terminals.

12.2.2.4 The modules should be kept in anti-static bags or other containers resistant to static for storage.

12.2.2.5 Only properly grounded soldering irons should be used.

12.2.2.6 If an electric screwdriver is used, it should be grounded and shielded to prevent sparks.

12.2.2.7 The normal static prevention measures should be observed for work clothes and working benches.

12.2.3.8 Since dry air is inductive to static, a relative humidity of 50-60% is recommended

12.2.3 Do not remove the panel or frame from the module.

12.2.4 The polarizing plate of the display is very fragile. Please handle it very carefully, do not touch, push or rub the exposed polarizing with anything harder than an HB pencil lead (glass, tweezers, etc.)

12.2.5 Do not wipe the polarizing plate with a dry cloth, as it may easily scratch the surface of plate.

12.2.6 Do not touch the display area with bare hands, this will stain the display area.

12.2.7 Do not use ketonics solvent & aromatic solvent. Use with a soft cloth soaked with a cleaning naphtha solvent.

12.2.8 To control temperature and time of soldering is $300 \pm 10^{\circ}\text{C}$ and 3-4 sec.

To avoid liquid (include organic solvent) stained on LCD Module.

12.3 STORAGE

12.3.1 Store the panel or module in a dark place where the temperature is $25^{\circ}\text{C} \pm 5^{\circ}\text{C}$ and the humidity is below 60% RH.

12.3.2 Avoid exposure to direct sunlight or to the light of fluorescent lamps.

12.3.3 Do not place the module near organic solvents or corrosive gases.

Do not crush, shake, or jolt the module.

12.4 LIMITED WARRANTY

12.4.1 FORMIKE modules are not consumer products, but may be incorporated by FORMIKE's customers into consumer products or components thereof, FORMIKE does not warrant that its modules and components are fit for any such particular purpose.

12.4.2 The liability of FORMIKE is limited to repair or replacement on the terms set forth below. FORMIKE will not be responsible for any subsequent or consequential events or injury or damage to any personnel or user including third party personnel and/or user. Unless otherwise agreed in writing between FORMIKE and the customer, FORMIKE will only replace or repair any of its Modules which is found defective electrically or visually when inspected in accordance with FORMIKE INSPECTION CRITERIA

12.4.3 No warranty can be granted if any of the precautions state in handling liquid crystal display has been disregarded. Broken glass, scratches on polarizer mechanical damages as well as defects that are caused accelerated environment tests are excluded from warranty.

12.4.4 In returning the modules, they must be properly packaged; there should be detailed description of the failures or defect.

13. OTHERS

13.1 If there is any not specified quality standard in this specification as well as RMA , please refer to < INSPECTION CRITERIA>. Contact FORMIKE to get the complete <INSPECTION CRITERIA> by the contact window or feedback@wandisplay.com.

13.2 Special agreement of <INSPECTION CRITERIA> is recognized only in writhing between FORMIKE and the customer also indicated it before ordering.