

**Module 1:
Introduction and Overview****7 pages**

- Summary of Features
- General Description
- Architecture
- Device/Package Combinations and Maximum I/O
- Ordering Examples

**Module 2:
Functional Description****41 pages**

- Detailed Description
 - Input/Output Blocks (IOBs)
 - Digitally Controlled Impedance (DCI)
 - Configurable Logic Blocks (CLBs)
 - 18-Kb Block SelectRAM™ Resources
 - 18-Bit x 18-Bit Multipliers
 - Global Clock Multiplexer Buffers
 - Digital Clock Manager (DCM)
- Routing
- Creating a Design
- Configuration

**Module 3:
DC and Switching Characteristics****43 pages**

- Electrical Characteristics
- Performance Characteristics
- Switching Characteristics
- Pin-to-Pin Output Parameter Guidelines
- Pin-to-Pin Input Parameter Guidelines
- DCM Timing Parameters
- Source-Synchronous Switching Characteristics

**Module 4:
Pinout Information****226 pages**

- Pin Definitions
- Pinout Tables
 - CS144/CSG144 Chip-Scale BGA Package
 - FG256/FGG256 Fine-Pitch BGA Package
 - FG456/FGG456 Fine-Pitch BGA Package
 - FG676/FGG676 Fine-Pitch BGA Package
 - BG575/BGG575 Standard BGA Package
 - BG728/BGG728 Standard BGA Package
 - FF896 Flip-Chip Fine-Pitch BGA Package
 - FF1152 Flip-Chip Fine-Pitch BGA Package
 - FF1517 Flip-Chip Fine-Pitch BGA Package
 - BF957 Flip-Chip BGA Package

IMPORTANT NOTE: *Page, figure, and table numbers begin at 1 for each module, and each module has its own Revision History at the end. Use the PDF "Bookmarks" pane for easy navigation in this volume.*

Summary of Virtex-II™ Features

- Industry First Platform FPGA Solution
- IP-Immersion Architecture
 - Densities from 40K to 8M system gates
 - 420 MHz internal clock speed (Advance Data)
 - 840+ Mb/s I/O (Advance Data)
- SelectRAM™ Memory Hierarchy
 - 3 Mb of dual-port RAM in 18 Kbit block SelectRAM resources
 - Up to 1.5 Mb of distributed SelectRAM resources
- High-Performance Interfaces to External Memory
 - DRAM interfaces
 - SDR / DDR SDRAM
 - Network FCRAM
 - Reduced Latency DRAM
 - SRAM interfaces
 - SDR / DDR SRAM
 - QDR™ SRAM
 - CAM interfaces
- Arithmetic Functions
 - Dedicated 18-bit x 18-bit multiplier blocks
 - Fast look-ahead carry logic chains
- Flexible Logic Resources
 - Up to 93,184 internal registers / latches with Clock Enable
 - Up to 93,184 look-up tables (LUTs) or cascadable 16-bit shift registers
 - Wide multiplexers and wide-input function support
 - Horizontal cascade chain and sum-of-products support
 - Internal 3-state bussing
- High-Performance Clock Management Circuitry
 - Up to 12 DCM (Digital Clock Manager) modules
 - Precise clock de-skew
 - Flexible frequency synthesis
 - High-resolution phase shifting
 - 16 global clock multiplexer buffers
- Active Interconnect Technology
 - Fourth generation segmented routing structure
 - Predictable, fast routing delay, independent of fanout
- SelectIO™-Ultra Technology
 - Up to 1,108 user I/Os
 - 19 single-ended and six differential standards
 - Programmable sink current (2 mA to 24 mA) per I/O
 - Digitally Controlled Impedance (DCI) I/O: on-chip termination resistors for single-ended I/O standards
- PCI-X compatible (133 MHz and 66 MHz) at 3.3V
- PCI compliant (66 MHz and 33 MHz) at 3.3V
- CardBus compliant (33 MHz) at 3.3V
- Differential Signaling
 - 840 Mb/s Low-Voltage Differential Signaling I/O (LVDS) with current mode drivers
 - Bus LVDS I/O
 - Lightning Data Transport (LDT) I/O with current driver buffers
 - Low-Voltage Positive Emitter-Coupled Logic (LVPECL) I/O
 - Built-in DDR input and output registers
- Proprietary high-performance SelectLink Technology
 - High-bandwidth data path
 - Double Data Rate (DDR) link
 - Web-based HDL generation methodology
- Supported by Xilinx Foundation™ and Alliance Series™ Development Systems
 - Integrated VHDL and Verilog design flows
 - Compilation of 10M system gates designs
 - Internet Team Design (ITD) tool
- SRAM-Based In-System Configuration
 - Fast SelectMAP configuration
 - Triple Data Encryption Standard (DES) security option (Bitstream Encryption)
 - IEEE 1532 support
 - Partial reconfiguration
 - Unlimited reprogrammability
 - Readback capability
- 0.15 µm 8-Layer Metal Process with 0.12 µm High-Speed Transistors
- 1.5V (V_{CCINT}) Core Power Supply, Dedicated 3.3V V_{CCAUX} Auxiliary and V_{CCO} I/O Power Supplies
- IEEE 1149.1 Compatible Boundary-Scan Logic Support
- Flip-Chip and Wire-Bond Ball Grid Array (BGA) Packages in Three Standard Fine Pitches (0.80 mm, 1.00 mm, and 1.27 mm)
- Wire-Bond BGA Devices Available in Pb-Free Packaging (www.xilinx.com/pbfree)
- 100% Factory Tested