

Chapter 1 Introduction

1.1 Overview

The RK809 is a complex power-management integrated circuit (PMIC) integrated CODEC for multi-core system applications powered by an external power supply. The RK809 can provide a complete power management solution with very few external components.

The RK809 provides five configurable synchronous step-down converters. The device also contains 9 LDO regulators, two switches and a battery fuel gauge. Power-up/power-down controller is configurable and can support any customized power-up/power-down sequences (OTP based). A real-time clock (RTC) is also integrated to provide a 32.768-kHz output buffer, and real time function. The RK809 supports 32.768-kHz clock generation based on a crystal oscillator. It also includes Audio CODEC , real ground Head phone driver and ClassD driver.

A "battery fuel gauge" is integrated in the RK809. Using the proprietary algorithms and the sensed battery current and voltage, the gauge can accurately calculate the battery capacity based on the charging/discharging characteristics of the battery preloaded in the system. The gauge then sends the battery capacity information to the processor through the I2C interface.

The RK809 can dynamically adjust the output voltage of each DC-DC converter, as required by the processor based on the processor's operation status so as to maximize the system efficiency. The output voltages of most channels can be configured through the I2C interface. The inputs of all channels have soft start function, which greatly reduces the inrush current at the startup.

The 2MHz switching frequency allows small size inductors to be used for both buck and boost converters. Also, as all the power switches are integrated on chip, no external power switches and Schottky diodes are needed, which reduces the system cost significantly.

The RK809 is available in a QFN68 7.0 mm x 7.0 mm package, with a 0.35-mm pin pitch.

1.2 Feature

- Input range: 2.7V - 5.5V
- Accurate battery fuel gauge with two separate battery voltage and current ADC
- Real time clock (RTC)
- Low standby current of 25uA (at 32.768KHz clock frequency)
- Real ground HeadPhone driver
- 1.3W ClassD PA without external filter inductor
- OTP Programmable power up/down sequences and voltage
- High performance Audio CODEC
 - One internal PLL
 - Support microphone input
 - Support I2S as the digital signal interface for both DAC and ADC
 - Support Automatic Level Control(ALC),limiter and noise gating
 - Support programmable digital and analog gains
 - Audio resolution from 16bits to 32bits
 - Sample rate up to 192KHz
 - Provides master and slave work mode, software configurable
 - Support 3 I2S formats (normal, left-justified, right-justified)
 - Support PDM mode(external input PCLK)
- Power channels:
 - ◆ CH1:Synchronous BUCK converter,2.5A max
 - ◆ CH2:Synchronous BUCK converter,2.5A max
 - ◆ CH3:Synchronous BUCK converter,1.5A max
 - ◆ CH4:Synchronous BUCK converter,1.5A max
 - ◆ CH5:Synchronous BUCK converter,2.5A max
 - ◆ CH6~CH7,CH9~CH14:LDOs, 400mA max
 - ◆ CH8:Low noise, high PSRR LDO,100mA max
 - ◆ CH15: Switch,1.5A max
 - ◆ CH16: Switch,3A max
- Package :7mmx7mm QFN68

1.3 Typical Application Diagrams

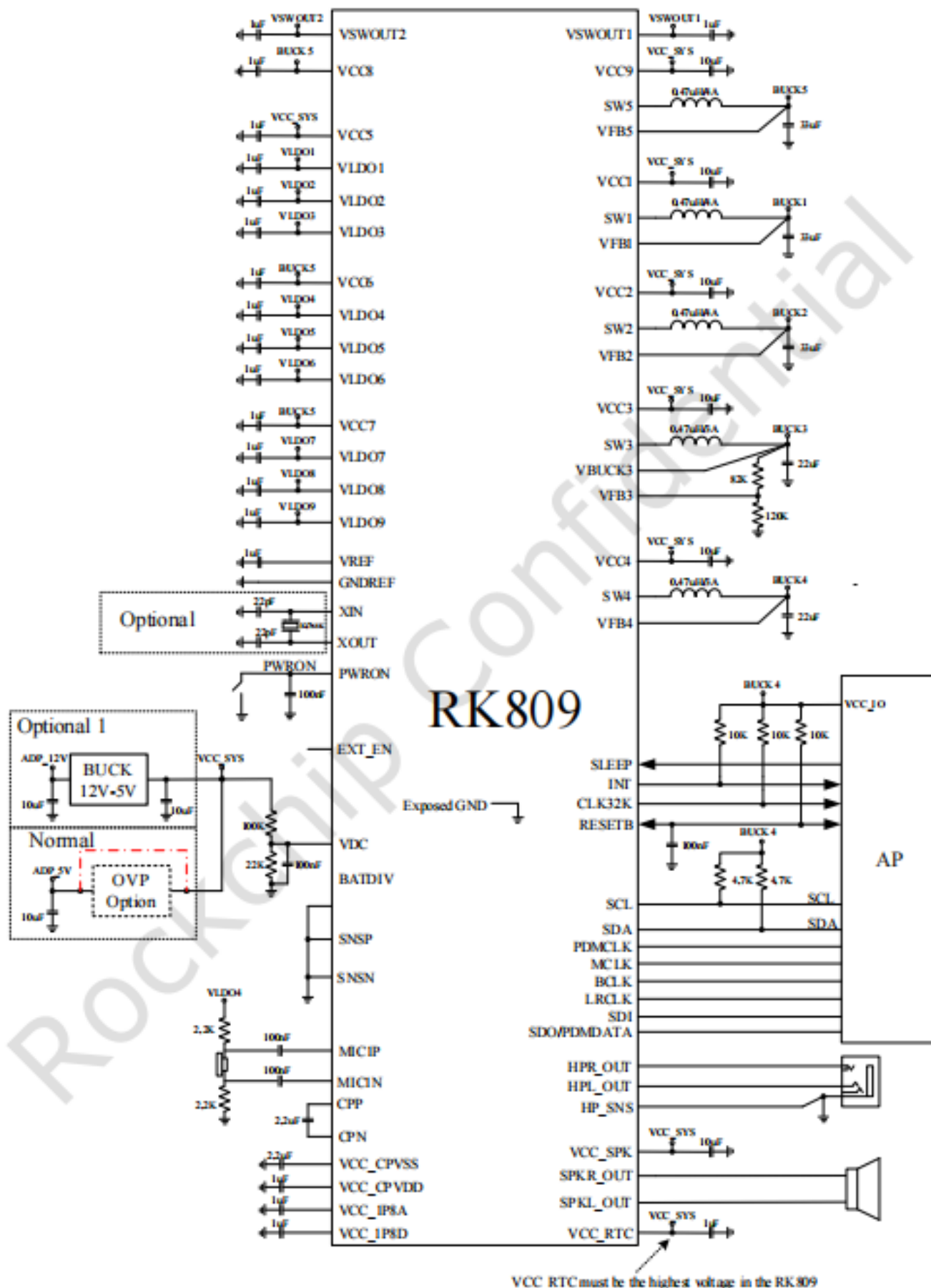


Fig. 1-1 RK809 Typical Application Diagram for no battery

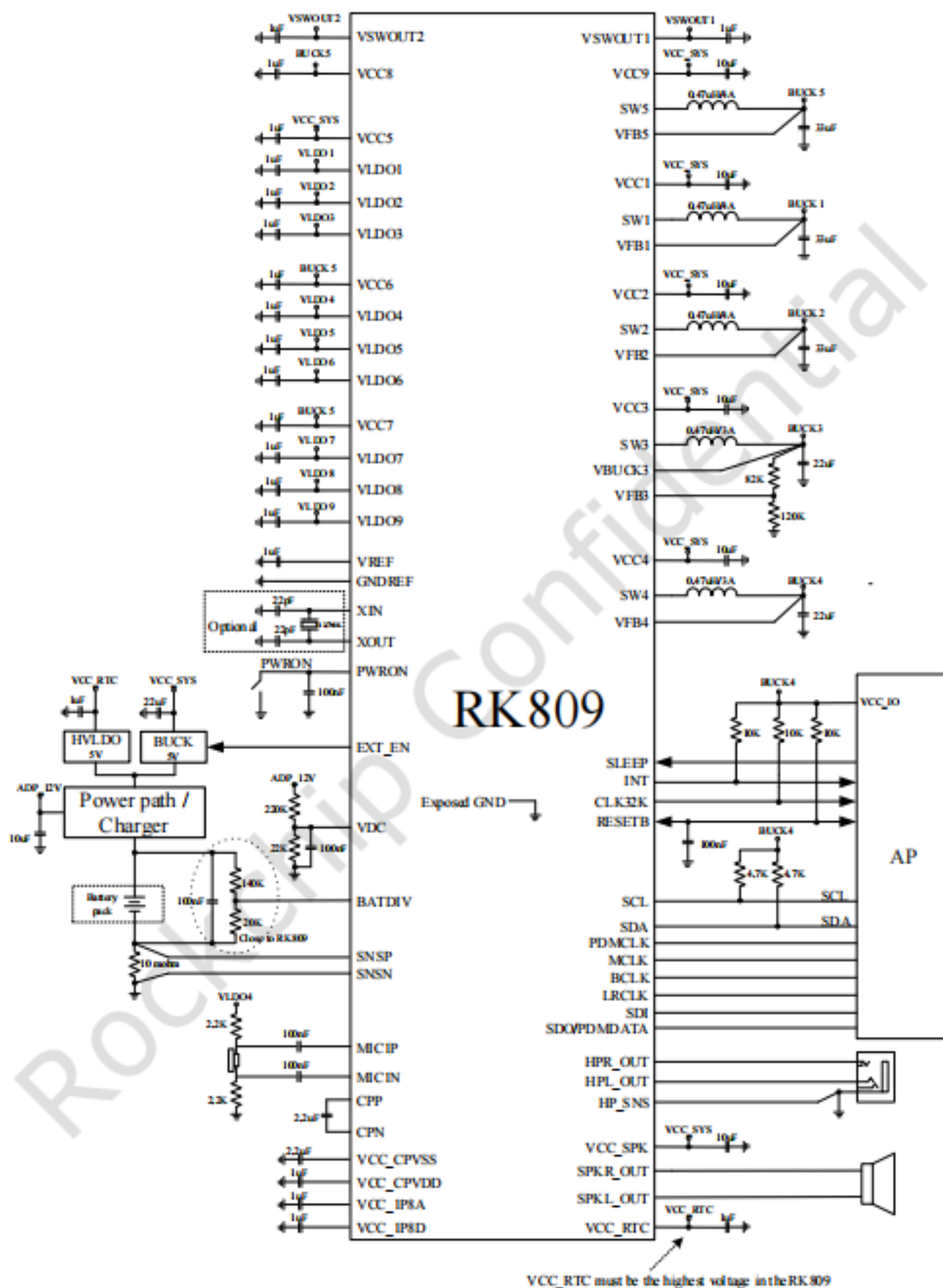


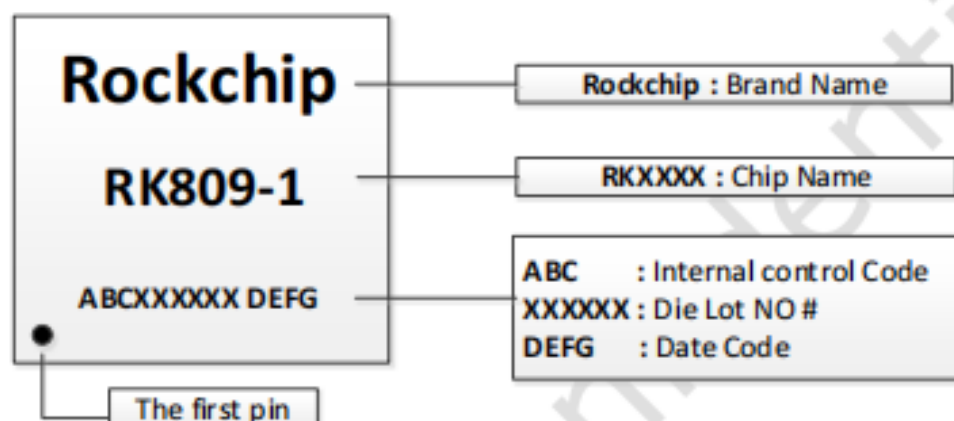
Fig. 1-2 RK809 Typical Application Diagram for two battery

Chapter 2 Package information

2.1 Ordering information

Orderable Device	RoHS status	Package	Package Detail
RK809-1	RoHS	QFN68 (7X7)	2000 pcs/ tape, 5 tapes/box

2.2 Top Marking



2.3 Dimension

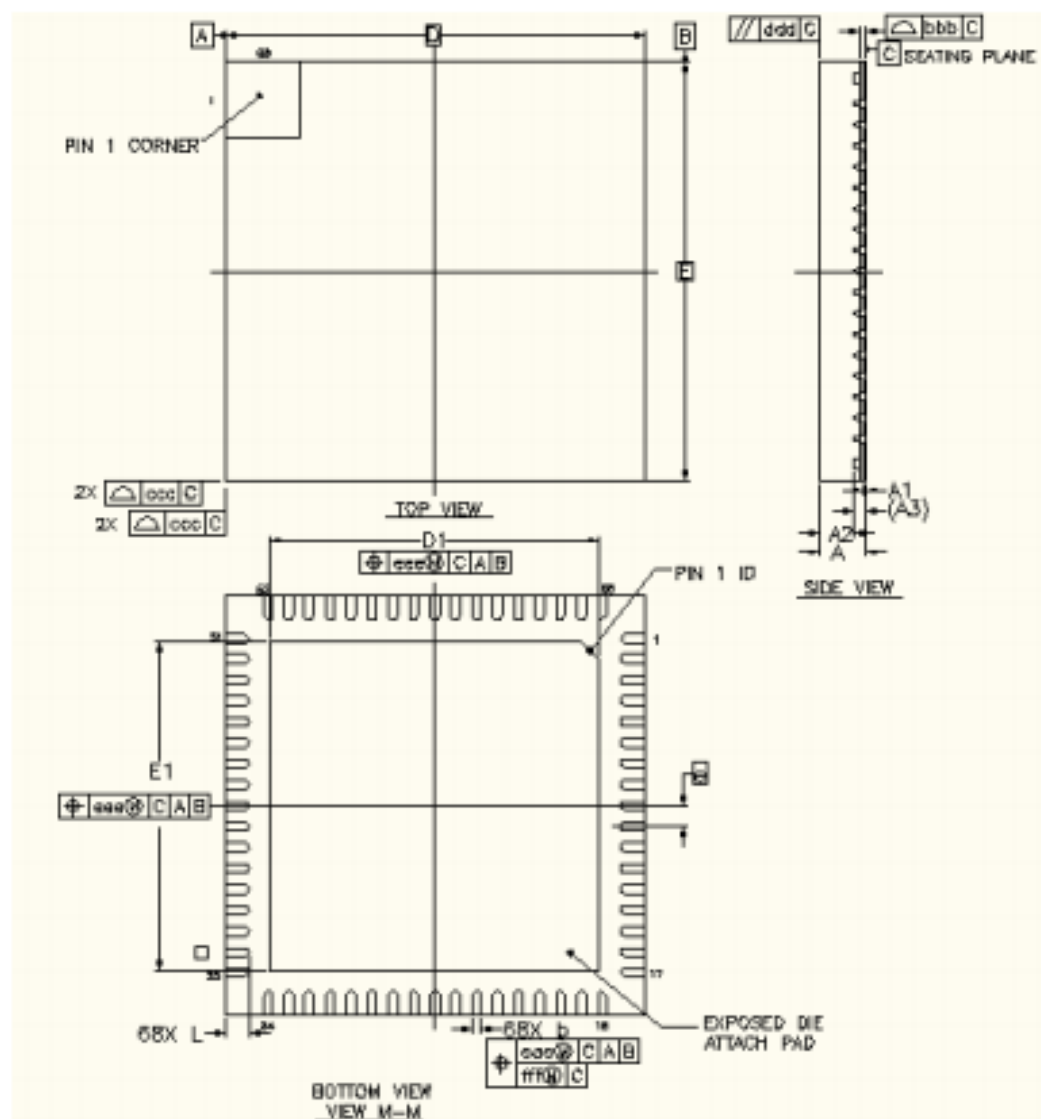


Fig. 2-1 QFN687mm X 7mm

DESCRIPTION	SYMBOL	MILLIMETER		
		MIN	NOM	MAX
TOTAL THICKNESS	A	0.70	0.75	0.80
STAND OFF	A1	0	0.035	0.05
MOLD THICKNESS	A2	-	0.55	0.57
MATERIAL THICKNESS	A3	-	0.203 _{REF}	-
PACKAGE SIZE	D	-	7 _{BSC}	-
	E	-	7 _{BSC}	-
EP SIZE	D1	5.39	5.49	5.59
	E1	5.39	5.49	5.59
LEAD LENGTH	L	0.30	0.4	0.50
LEAD PITCH	e	0.35 _{BSC}		
LEAD WIDTH	b	0.1	0.15	0.2
LEAD POSITION OFFSET	aaa	0.07		
LEAD COPLANARITY	bbb	0.08		
PACKAGE EDGE PROFILE	ccc	0.10		
MOLD FLATNESS	ddd	0.10		
EP POSITION OFFSET	eee	0.10		
	fff	0.05		

Note:

1. Coplanarity applies to leads, corner leads and die attach pad.
2. Dimension b applies to metalized terminal and is measured between 0.15mm and 0.30mm from the

terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension *b* should not be measure in that radius area.

2.4 Pin Assignment

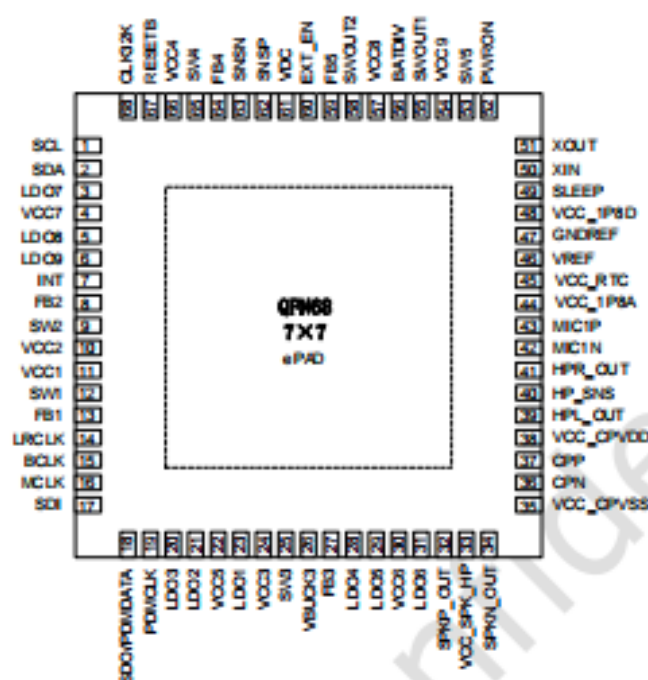


Fig. 2-2 Pin Assignment QFN7x7-68(Pitch=0.35mm)

2.5 Pinout Number Order

PIN NO	PIN NAME	PIN DESCRIPTION
1	SCL	I2C clock input
2	SDA	I2C data input and output
3	LDO7	LDO7 output
4	VCC7	Power supply of LDO7/8/9
5	LDO8	LDO8 output
6	LDO9	LDO9 output
7	INT	Interrupt request pin, open drain
8	FB2	Output feedback voltage of buck2
9	SW2	Switching node of buck2
10	VCC2	Power supply of buck2
11	VCC1	Power supply of buck1
12	SW1	Switching node of buck1
13	FB1	Output feedback voltage of buck1
14	LRCLK	The I2S framing clock
15	BCLK	The I2S bit clock
16	MCLK	The I2S main clock input pin
17	SDI	The I2S DAC input data
18	SDO/PDM DATA	The I2S ADC output data/PDM Data for the DSADC
19	PDMCLK	PDM CLK for the DSADC OUTPUT
20	LDO3	LDO3 output
21	LDO2	LDO2 output
22	VCC5	Power supply of LDO1/2/3
23	LDO1	LDO1 output