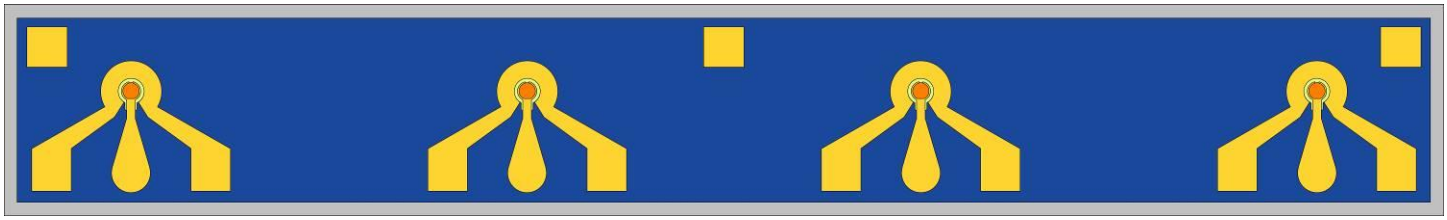


(P/N: XSJ-10-D6A-20-K4-750)

Introduction

This 4X25Gbps Array 100Gbps photodiode chip, which is top-illuminated and mesa structure high data rate digital PIN photodiode chip, active area size is Φ20μm. Its features is high, low capacitance, low dark current and excellent reliability, mainly combination with high performance 4X25Gbps quad channel transimpedance amplifiers(TIA), application in long wavelength applications, high date rate up to 4X25Gbps with single mode fiber optical receiver.

Features

1. Φ20μm active area.
2. Ground-Signal-Ground (GSG) bond pad structure, 4X25G array.
3. Low dark current, low capacitance, high responsibility.
4. Date rate: ≥ 25Gbps/channel.
5. Die pitch: 750μm.
6. Excellent reliability: All chips have passed the qualification requirements as specified by Telcordia -GR-468-CORE.
7. 100% testing and inspection.

Applications

1. IEEE 100 Gigabit Ethernet
2. 100G CWDM4,PSM4,CLR4
3. 100G(4X25Gbps) links
4. Single mode datacom and telecom
5. Fiber-optic transceivers, receiver and transponders

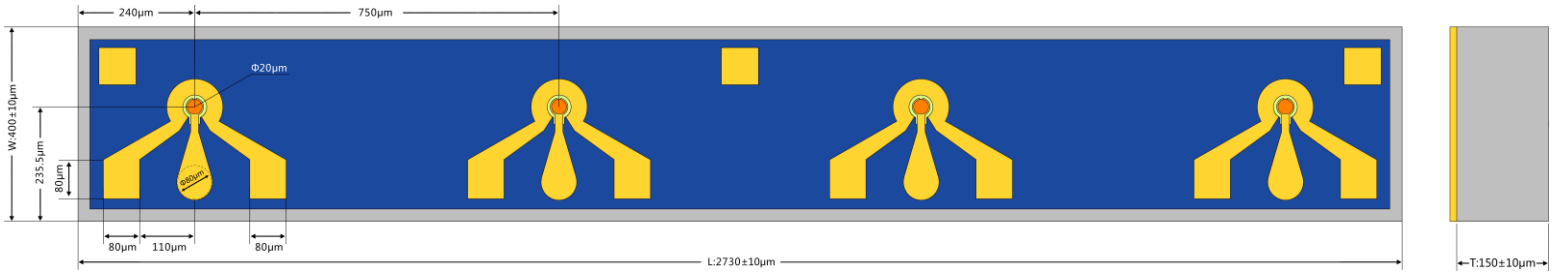
Electro-Optical characteristics (T_{op}=22±3℃, unless otherwise specified)

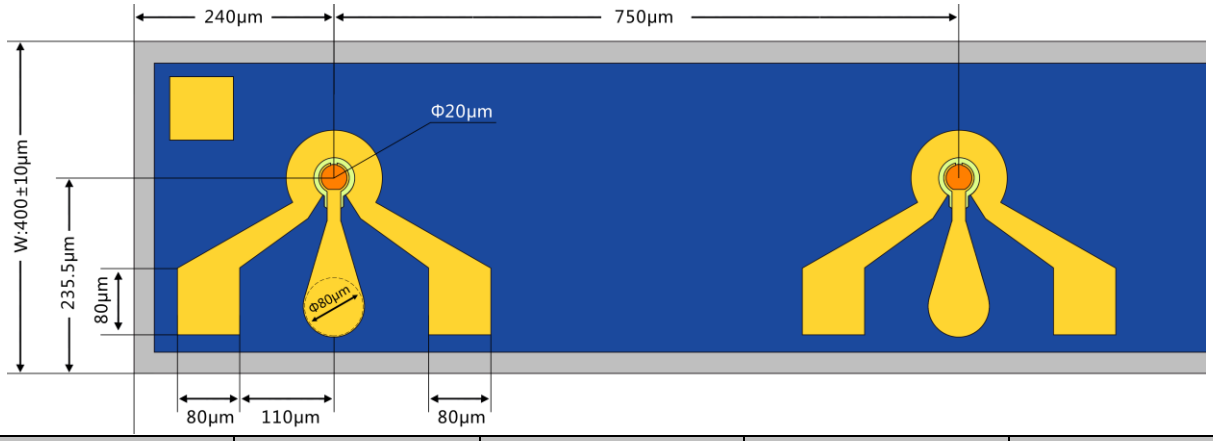
Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Response Spectrum	λ	910	1310/1550	1650	nm	
Dark Current	I_d		0.05	3.0	nA	V_R=5.0V
Reverse Breakdown Voltage	V_{BR}	30			V	I_R=10μA
Responsivity	*Re*	0.7			A/W	λ=1310nm P_{in}=0.5mW, V_R=1.0V
Bandwidth	*BW*		22		GHz	λ=1550nm@-3dB, R_L=50Ω P_{in}= 0.5mW, V_R=2.0V
Capacitance	C_j		0.08	0.1	pF	f=1MHz, V_R=5.0V

Absolute Maximum Rating

Parameter	Symbol	Min.	Max.	Unit
Reverse Voltage	V_R		10	V
Forward Current	I_F		10	mA
Reverse Current	I_R		5	mA
Optical Power Input	P_{in}		10	mW
Storage Temperature	T_{stg}	-45	125	℃
Operating Temperature	T_{op}	-40	85	℃

Dimensions





	Min.	Typ.	Max.	Unit
Active Area		Φ20		μm
Signal Bond Pad		Φ80		μm
Ground Bond Pad(Both)		80X80		μm
Die Length	2720	2730	2740	μm
Die Width	390	400	410	μm
Die Height	140	150	160	μm
Die Pitch		750		μm

Cautions

1. Take necessary ESD protective measures, avoid to prevent electrostatic damage the chip.
2. InP-based chip are easily fragile and damaged, should be very carefully used when handling.
3. Do not handle with tweezers, recommended by vacuum adsorption.
4. Bonding force, temperature should be carefully setting, in order to avoid damage to the chip.