

RF Agile Transceiver

FEATURES

- ▶ RF 2 × 2 transceiver with integrated 12-bit DACs and ADCs
- ▶ TX band: 47 MHz to 6.0 GHz
- ▶ RX band: 70 MHz to 6.0 GHz
- ▶ Supports TDD and FDD operation
- ▶ Tunable channel bandwidth: <200 kHz to 56 MHz
- ▶ Dual receivers: 6 differential inputs
- ▶ Superior receiver sensitivity with a noise figure of 2 dB at 800 MHz LO
- ▶ RX gain control
 - ▶ Real-time monitor and control signals for manual gain
 - ▶ Independent automatic gain control
- ▶ Dual transmitters: 4 differential outputs
- ▶ Highly linear broadband transmitter
 - ▶ TX EVM: ≤-40 dB
 - ▶ TX noise: ≤-157 dBm/Hz noise floor
 - ▶ TX monitor: ≥66 dB dynamic range with 1 dB accuracy
- ▶ Integrated fractional-N synthesizers
 - ▶ 2.4 Hz maximum local oscillator (LO) step size
- ▶ Multichip synchronization
- ▶ CMOS/LVDS digital interface

APPLICATIONS

- ▶ Point to point communication systems
- ▶ Femtocell/picocell/microcell base stations
- ▶ General-purpose radio systems

GENERAL DESCRIPTION

The AD9361 is a high performance, highly integrated radio frequency (RF) Agile Transceiver™ designed for use in 3G and 4G base station applications. Its programmability and wideband capability make it ideal for a broad range of transceiver applications. The device combines a RF front end with a flexible mixed-signal baseband section and integrated frequency synthesizers, simplifying design-in by providing a configurable digital interface to a processor. The AD9361 receiver LO operates from 70 MHz to 6.0 GHz and the transmitter LO operates from 47 MHz to 6.0 GHz range, covering most licensed and unlicensed bands. Channel bandwidths from less than 200 kHz to 56 MHz are supported.

The two independent direct conversion receivers have state-of-the-art noise figure and linearity. Each receive (RX) subsystem includes independent automatic gain control (AGC), dc offset correction, quadrature correction, and digital filtering, thereby eliminating the need for these functions in the digital baseband. The AD9361 also has flexible manual gain modes that can be externally controlled. Two high dynamic range analog-to-digital converters (ADCs) per channel digitize the received I and Q signals and pass them through configurable decimation filters and 128-tap finite impulse response (FIR) filters to produce a 12-bit output signal at the appropriate sample rate.

The transmitters use a direct conversion architecture that achieves high modulation accuracy with ultralow noise. This transmitter design produces a best in class TX error vector magnitude (EVM) of <-40 dB, allowing significant system margin for the external power amplifier (PA) selection. The on-board transmit (TX) power monitor can be used as a power detector, enabling highly accurate TX power measurements.

The fully integrated phase-locked loops (PLLs) provide low power fractional-N frequency synthesis for all receive and transmit channels. Channel isolation, demanded by frequency division duplex (FDD) systems, is integrated into the design. All VCO and loop filter components are integrated.

The core of the AD9361 can be powered directly from a 1.3 V regulator. The IC is controlled via a standard 4-wire serial port and four real-time input/output control pins. Comprehensive power-down modes are included to minimize power consumption during normal use. The AD9361 is packaged in a 10 mm × 10 mm, 144-ball chip scale package ball grid array (CSP_BGA).

TABLE OF CONTENTS

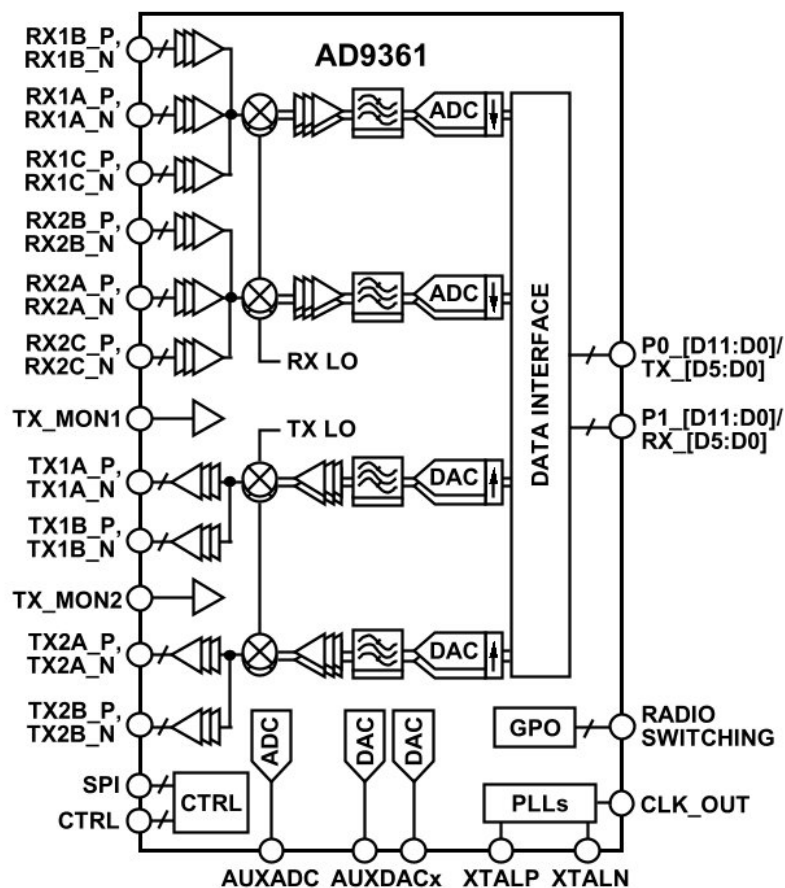
Features.....	1	Theory of Operation.....	35
Applications.....	1	General.....	35
General Description.....	1	Receiver.....	35
Functional Block Diagram.....	3	Transmitter.....	35
Specifications.....	4	Clock Input Options.....	35
Current Consumption—VDD_Interface.....	10	Synthesizers.....	36
Current Consumption—VDDD1P3_DIG and		Digital Data Interface.....	36
VDDAx (Combination of All 1.3 V Supplies)...	12	Enable State Machine.....	36
Absolute Maximum Ratings.....	17	SPI Interface.....	37
Reflow Profile.....	17	Control Pins.....	37
Thermal Resistance.....	17	GPO Pins (GPO_3 to GPO_0).....	37
ESD Caution.....	17	Auxiliary Converters.....	37
Pin Configuration and Function Descriptions.....	18	Powering the AD9361.....	37
Typical Performance Characteristics.....	22	Packaging and Ordering Information.....	39
800 MHz Frequency Band.....	22	Outline Dimensions.....	39
2.4 GHz Frequency Band.....	27	Ordering Guide.....	39
5.5 GHz Frequency Band.....	31	Evaluation Boards.....	39

REVISION HISTORY

3/2024—Rev. F to Rev. G

Changed Slave to Subordinate (Throughout).....	1
Changes to Features Section.....	1
Moved Figure 1.....	3
Changes to Input Parameter, Table 1.....	4
Change to Clock Input Options Section.....	35
Added Evaluation Boards.....	39

FUNCTIONAL BLOCK DIAGRAM



NOTES

1. SPI, CTRL, P0 [D11:D0]/TX [D5:D0], P1 [D11:D0]/RX [D5:D0], AND RADIO SWITCHING CONTAIN MULTIPLE PINS.

001

Figure 1.

SPECIFICATIONS

Electrical characteristics at VDD_GPO = 3.3 V, VDD_INTERFACE = 1.8 V, and all other VDDx pins = 1.3 V, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter ¹	Symbol	Min	Typ	Max	Unit	Test Conditions/ Comments
RECEIVERS, GENERAL						
Center Frequency		70		6000	MHz	
Gain						
Minimum			0		dB	
Maximum			74.5		dB	At 800 MHz
			73.0		dB	At 2300 MHz (RX1A, RX2A)
			72.0		dB	At 2300 MHz (RX1B, RX1C, RX2B, RX2C)
			65.5		dB	At 5500 MHz (RX1A, RX2A)
Gain Step			1		dB	
Received Signal Strength Indicator	RSSI					
Range			100		dB	
Accuracy			±2		dB	
RECEIVERS, 800 MHz						
Noise Figure	NF		2		dB	Maximum RX gain
Third-Order Input Intermodulation Intercept Point	IIP3		-18		dBm	Maximum RX gain
Second-Order Input Intermodulation Intercept Point	IIP2		40		dBm	Maximum RX gain
Local Oscillator (LO) Leakage			-122		dBm	At RX front-end input
Quadrature						
Gain Error			0.2		%	
Phase Error			0.2		Degrees	
Modulation Accuracy (EVM)			-42		dB	19.2 MHz reference clock
Input S ₁₁			-10		dB	
RX1 to RX2 Isolation						
RX1A to RX2A, RX1C to RX2C			70		dB	
RX1B to RX2B			55		dB	
RX2 to RX1 Isolation						
RX2A to RX1A, RX2C to RX1C			70		dB	
RX2B to RX1B			55		dB	
RECEIVERS, 2.4 GHz						
Noise Figure	NF		3		dB	Maximum RX gain
Third-Order Input Intermodulation Intercept Point	IIP3		-14		dBm	Maximum RX gain
Second-Order Input Intermodulation Intercept Point	IIP2		45		dBm	Maximum RX gain
LO Leakage			-110		dBm	At receiver front-end input
Quadrature						
Gain Error			0.2		%	
Phase Error			0.2		Degrees	
Modulation Accuracy (EVM)			-42		dB	40 MHz reference clock
Input S ₁₁			-10		dB	
RX1 to RX2 Isolation						
RX1A to RX2A, RX1C to RX2C			65		dB	