

REPORT · SEPTEMBER 2026

# CMOS Image Sensor

1/2.8-inch 5 MP Back-Illuminated CMOS Image Sensor - Technical  
Datasheet

# 1. Product Description

The IS-5280 is a 1/2.8-inch optical format, 5.17 megapixel back-illuminated (BSI) CMOS image sensor with a 2.0 µm pixel pitch. It targets cost-sensitive but image-quality-critical designs such as security IP cameras, dash cams, USB/UVC webcams and entry-level machine vision. The sensor integrates a 12-bit column-parallel ADC, an on-chip PLL, a MIPI CSI-2 transmitter and a two-wire serial control interface on a single die, so the host needs only one master clock, one reset line and one I2C bus to bring up a complete camera pipeline.

The back-illuminated pixel structure places the metal routing behind the photodiode, which raises quantum efficiency and reduces crosstalk at oblique incidence. In practice this means better low-light sensitivity and less colour shading with short CRA lenses than a front-illuminated part of the same pixel size. The device is supplied either as a bare die for COB assembly or in a CSP package; both share the same electrical interface and register set.

**Positioning - a mainstream 5 MP, 2.0 µm BSI sensor for the mid-tier security and automotive-recorder market: the volume sweet spot where 1/2.8-inch lenses, 5 MP resolution and MIPI output are already the default system design.**

# 2. Product Identification

| Item             | Value                        | Notes                                               |
|------------------|------------------------------|-----------------------------------------------------|
| Brand            | [BRAND]                      | Replace with your own brand before publishing       |
| Model / Part No. | IS-5280                      | Placeholder - replace with the real part number (*) |
| SKU / Variant    | IS-5280-BSI-5MP-MIPI         | Placeholder (*)                                     |
| Sensor type      | CMOS, back-illuminated (BSI) | (*)                                                 |
| Optical format   | 1/2.8 inch                   | (*)                                                 |

| Item              | Value                                     | Notes                                             |
|-------------------|-------------------------------------------|---------------------------------------------------|
| Active array      | 2880 x 1808 (5.17 MP)                     | (*)                                               |
| Pixel size        | 2.0 $\mu\text{m}$ x 2.0 $\mu\text{m}$     | (*)                                               |
| Shutter type      | Electronic rolling shutter                | (*)                                               |
| Output            | MIPI CSI-2, 2-lane / 4-lane, RAW10 / RAW8 | (*)                                               |
| Control           | I2C, 16-bit register address              | (*)                                               |
| Delivery form     | CSP package / bare die (COB)              | (*)                                               |
| Country of origin | [COUNTRY]                                 | Must match the actual production site for customs |

## 3. Key Features

- 1/2.8-inch BSI CMOS, 5.17 MP active array (2880 x 1808), 2.0  $\mu\text{m}$  pixel
- 12-bit on-chip column-parallel ADC, output packed as RAW10 or RAW8
- MIPI CSI-2 output, 1 / 2 / 4 data lanes, up to 1500 Mbps per lane (\*)
- On-chip PLL - a single 24 MHz master clock is sufficient for all internal timing
- Programmable exposure and analog/digital gain through the I2C control bus
- Horizontal mirror, vertical flip, 2x2 binning and windowed (ROI) readout
- Embedded test pattern generator for interface bring-up and debugging
- Low power: approximately 115 mW in 1080p30 mode, below 10  $\mu\text{A}$  in software standby (\*)
- On-chip OTP memory for module calibration data such as lens shading and defect maps (\*)

## 4. Applications

- Security IP cameras and network video recorders (1080p / 3 MP / 5 MP)
- Automotive dash cams and rear-view cameras

- USB / UVC webcams and video conference cameras
- Entry-level machine vision, barcode readers and document scanners
- Smart doorbells, baby monitors and robotic vacuums
- Embedded vision on single-board computers with a MIPI CSI-2 host port

## 5. Standards and Compliance

| Area                 | Standard / Requirement                         | Status                                         |
|----------------------|------------------------------------------------|------------------------------------------------|
| RoHS                 | Directive (EU) 2011/65 plus amendment 2015/863 | Compliant (*)                                  |
| REACH                | Regulation (EC) 1907/2006, SVHC candidate list | Compliant (*)                                  |
| Halogen-free         | IEC 61249-2-21                                 | Compliant (*)                                  |
| Moisture sensitivity | J-STD-020 / J-STD-033, MSL 3                   | Per package variant (*)                        |
| ESD                  | ANSI/ESDA/JEDEC JS-001 (HBM), JS-002 (CDM)     | See Section 16 (*)                             |
| Reliability          | JESD22 / JESD47 test family                    | See Section 16 (*)                             |
| Automotive grade     | AEC-Q100                                       | Not qualified by default - only if ordered (*) |

Compliance status must be re-confirmed against the certificates issued for the exact production lot and package variant. Never copy a compliance claim from another sensor model or another supplier.

## 6. Absolute Maximum Ratings

Stresses beyond the values below may cause permanent damage. These are stress ratings only; operation outside the recommended operating conditions is not implied.

| Parameter                   | Symbol | Min  | Max | Unit |
|-----------------------------|--------|------|-----|------|
| Analog supply voltage       | AVDD   | -0.3 | 2.1 | V    |
| Digital core supply voltage | DVDD   | -0.3 | 1.5 | V    |

| Parameter                      | Symbol  | Min  | Max         | Unit  |
|--------------------------------|---------|------|-------------|-------|
| I/O supply voltage             | DOVDD   | -0.3 | 3.6         | V     |
| Input voltage, any digital pin | VIN     | -0.3 | DOVDD + 0.3 | V     |
| Storage temperature            | Tstg    | -40  | +125        | deg C |
| Operating junction temperature | Tj      | -30  | +100        | deg C |
| Electrostatic discharge, HBM   | ESD_HBM | -    | 2000        | V     |
| Electrostatic discharge, CDM   | ESD_CDM | -    | 500         | V     |
| Reflow peak temperature        | Tpeak   | -    | 260         | deg C |

## 7. Recommended Operating Conditions

| Parameter                         | Min  | Typ  | Max  | Unit  |
|-----------------------------------|------|------|------|-------|
| Analog supply AVDD                | 2.7  | 2.8  | 2.9  | V     |
| Digital core supply DVDD          | 1.14 | 1.20 | 1.26 | V     |
| I/O supply DOVDD                  | 1.7  | 1.8  | 3.3  | V     |
| MIPI PHY supply, if separate      | 1.14 | 1.20 | 1.26 | V     |
| Master clock input MCLK           | 6    | 24   | 27   | MHz   |
| Operating ambient temperature (*) | -30  | 25   | +85  | deg C |
| I2C clock frequency               | -    | -    | 400  | kHz   |
| MIPI lane data rate, per lane     | -    | -    | 1500 | Mbps  |

(\*) The ambient range applies to the CSP variant. Bare-die COB modules must be qualified together with the module substrate and lens holder, because the module thermal path, not the die alone, sets the achievable ambient limit. Confirm the rating on the final assembled module before publishing it.

## 8. Optical and Image Characteristics

| Parameter                    | Typical     | Unit     | Notes                             |
|------------------------------|-------------|----------|-----------------------------------|
| Active pixels                | 2880 x 1808 | pixels   | 16:10 aspect, 5.17 MP             |
| Optical format               | 1/2.8       | inch     | Image circle diagonal 6.51 mm (*) |
| Pixel size                   | 2.0 x 2.0   | µm       | BSI structure (*)                 |
| Full well capacity           | 8000        | e-       | At conversion gain 1x (*)         |
| Sensitivity                  | 3000        | mV/lux-s | At 550 nm, 1x gain (*)            |
| Signal-to-noise ratio        | 40          | dB       | Maximum, 1x gain (*)              |
| Dynamic range, linear        | 72          | dB       | Single exposure (*)               |
| Dark current                 | 30          | e-/s     | At 25 deg C (*)                   |
| Dark current doubling        | 6 to 8      | deg C    | Typical junction behaviour (*)    |
| Chief ray angle, CRA         | 20          | deg      | Lens must be CRA matched (*)      |
| Quantum efficiency at 550 nm | 78          | %        | With IR-cut filter removed (*)    |
| Parasitic light sensitivity  | -85         | dB       | (*) measured with lens in place   |

All optical values above are typical reference figures for a BSI 2.0 µm pixel of this class. They are not measured data for a specific production lot and must be replaced with measured values before this document is used in a quotation, a listing or a customer datasheet.

## 9. Sensor Architecture and Scan Modes

The signal chain is deliberately simple: photons are converted in the pixel array, digitised by a column-parallel 12-bit ADC, packed by the digital block and transmitted over MIPI CSI-2 to the host SoC. Sensor configuration (exposure, gain, window, lane count) travels on a separate I2C path, so the control bus and the high-speed data path are independent.

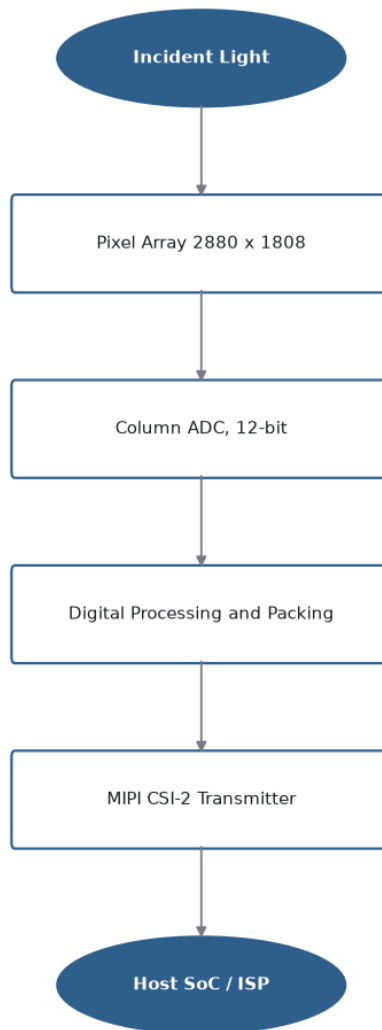


Figure 1: Simplified signal chain from incident light to host SoC. The I2C control path and the clock / PLL block run in parallel and are omitted for clarity.

## 9.1 Resolution and Frame Rate

| Output size      | Active pixels | Max frame rate | Interface       |
|------------------|---------------|----------------|-----------------|
| 5 MP, full array | 2880 x 1808   | 30 fps         | MIPI 2-lane (*) |
| 3 MP             | 2304 x 1296   | 45 fps         | MIPI 2-lane (*) |
| 1080p            | 1920 x 1080   | 60 fps         | MIPI 2-lane (*) |
| 720p             | 1280 x 720    | 90 fps         | MIPI 1-lane (*) |

Frame rates are typical and depend on the MIPI lane count, the PLL settings, the exposure time and the host's ability to consume the stream. The achievable frame rate must be measured on the final module, in the final mode, before it is quoted to a customer.

## 9.2 Readout Modes

- Full-resolution rolling-shutter readout with programmable integration time
- Windowed ROI readout, which raises the frame rate at the cost of field of view
- 2x2 binning for roughly four times the sensitivity at half resolution
- Horizontal mirror and vertical flip, combinable with ROI windowing
- Test pattern generator for interface bring-up and lane-lock debugging

# 10. Output Interface and Data Formats

| Parameter            | Specification                            | Notes                               |
|----------------------|------------------------------------------|-------------------------------------|
| High-speed interface | MIPI CSI-2, D-PHY                        | (*)                                 |
| Data lanes           | 1 / 2 / 4, pin and register configurable | (*)                                 |
| Maximum lane rate    | 1500 Mbps per lane                       | (*)                                 |
| Pixel data formats   | RAW10, RAW8; 12-bit internal             | (*) Bayer order must be confirmed   |
| Control interface    | I2C, up to 400 kHz                       | 16-bit register address, 8-bit data |
| I2C device address   | 0x6C (7-bit) / 0x36 (8-bit write)        | (*)                                 |

| Parameter          | Specification         | Notes                          |
|--------------------|-----------------------|--------------------------------|
| Reset / power-down | XSHUTDOWN, active low | (*) hold low for at least 1 ms |

## 11. Electrical Characteristics

| Rail             | Nominal | Typical current  | Notes                        |
|------------------|---------|------------------|------------------------------|
| Analog supply    | 2.8 V   | 25 mA            | (*) measured in 1080p30      |
| Digital core     | 1.2 V   | 45 mA            | (*)                          |
| I/O supply       | 1.8 V   | 15 mA            | (*) no heavy I/O load        |
| MIPI PHY         | 1.2 V   | 30 mA            | (*) two active lanes         |
| Software standby | -       | below 10 $\mu$ A | (*) clock stopped, I2C alive |

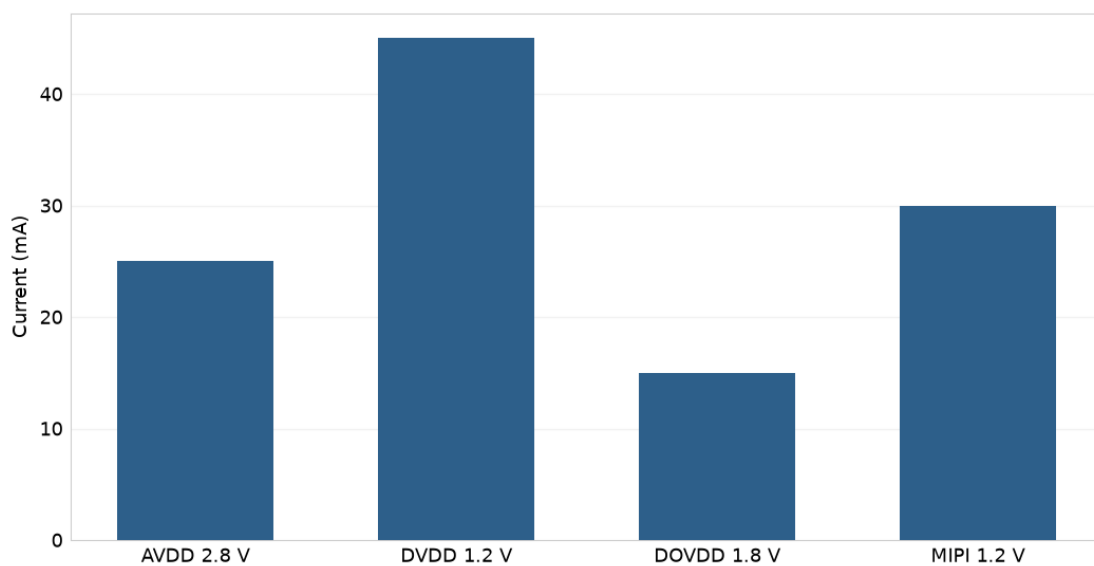


Figure 2: Typical supply current by rail in 1080p30 mode. Indicative values - confirm by measurement on the final module.

Total module power is dominated by the digital core and the MIPI PHY. When budgeting power for a battery-powered design, add the LED illuminator and the ISP separately; they usually exceed the sensor by a large margin.

# 12. Clock, Timing and Control Interface

| Item                  | Value                            | Notes                                  |
|-----------------------|----------------------------------|----------------------------------------|
| Master clock MCLK     | 24 MHz                           | (*) 6 to 27 MHz supported              |
| On-chip PLL           | Yes                              | Generates pixel and MIPI clocks        |
| Reset                 | XSHUTDOWN, active low            | Hold low for at least 1 ms at power-up |
| I2C address           | 0x6C / 0x36                      | 7-bit / 8-bit write                    |
| Register width        | 16-bit address, 8-bit data       | (*) per register map                   |
| Frame synchronisation | Free-running or external trigger | (*) optional trigger input             |

# 13. Register Interface Overview

Configuration is written over I2C as 16-bit register addresses with 8-bit data. The sequence below is a minimal bring-up order; the real register map must always be taken from the manufacturer's official documentation for the exact silicon revision.

TEXT

```
# Minimal bring-up sequence (pseudo register map)
# 1. Release reset
write(0x6C, 0x0103, 0x01)    # software reset
sleep(20 ms)
# 2. Clock / PLL enable
write(0x6C, 0x0301, 0x01)
# 3. MIPI: two lanes, RAW10
write(0x6C, 0x4501, 0x02)
# 4. Stream on
write(0x6C, 0x0100, 0x01)
# 5. Read back a known ID register to confirm the link
id = read(0x6C, 0x300A)
```

## 13.1 Key Register Groups

| Address block   | Function                                       |
|-----------------|------------------------------------------------|
| 0x0100 - 0x0103 | Mode select, stream on and off, software reset |
| 0x0300 - 0x0310 | PLL and system clock dividers                  |
| 0x3500 - 0x3512 | Exposure time and analog / digital gain        |
| 0x3800 - 0x3810 | Window, crop and output size                   |
| 0x4500 - 0x4510 | MIPI lane count, data type and timing          |

## 14. Spectral Response and Performance Curves

The curve below is the typical relative quantum efficiency of a back-illuminated 2.0  $\mu\text{m}$  pixel with the IR-cut filter removed. With a standard IR-cut filter fitted, the response above about 650 nm is strongly attenuated.

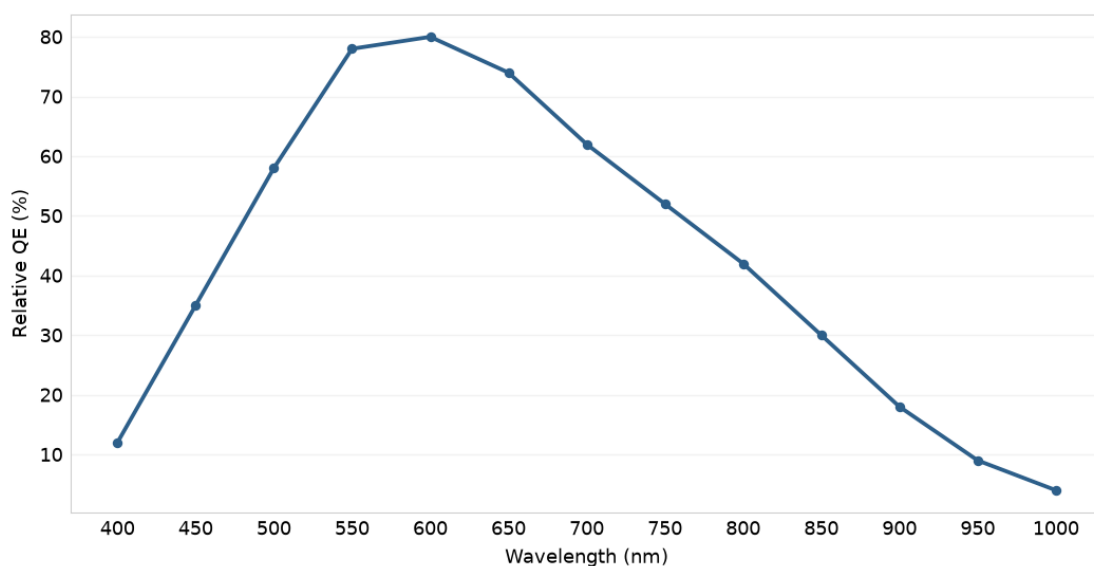


Figure 3: Typical relative quantum efficiency versus wavelength, BSI pixel without IR-cut filter. Indicative only - replace with measured data.

**Only the variant supplied without an IR-cut filter should be marketed as NIR sensitive. Claiming 850 nm or 940 nm performance on an IR-cut module is one of the most common returns in this category.**

## 15. Package and Mechanical

| Parameter          | Value                                     | Notes                                     |
|--------------------|-------------------------------------------|-------------------------------------------|
| Package options    | CSP / bare die (COB)                      | (*)                                       |
| CSP outline        | approximately 6.0 x 4.5 x 0.8 mm          | (*)                                       |
| Pad / ball count   | [N]                                       | Confirm against the final package drawing |
| Optical centre     | [x, y] from package datum                 | (*) required for lens alignment           |
| Cover              | Glass lid (CSP) / clear encapsulant (COB) | (*)                                       |
| Die tilt tolerance | [spec]                                    | (*) define together with the module maker |

### 15.1 Pad / Pin Description (CSP, representative)

| Pin | Name  | Type   | Function                  |
|-----|-------|--------|---------------------------|
| A1  | AVDD  | Power  | 2.8 V analog supply       |
| A2  | AGND  | Ground | Analog ground             |
| B1  | DVDD  | Power  | 1.2 V digital core supply |
| B2  | DGND  | Ground | Digital ground            |
| C1  | DOVDD | Power  | 1.8 V I/O supply          |
| C2  | SCL   | I/O    | I2C clock                 |
| D1  | SDA   | I/O    | I2C data                  |
| D2  | MCLK  | Input  | Master clock input        |

| Pin | Name        | Type   | Function               |
|-----|-------------|--------|------------------------|
| E1  | MDP0 / MDN0 | Output | MIPI data lane 0       |
| E2  | MDP1 / MDN1 | Output | MIPI data lane 1       |
| F1  | XSHUTDOWN   | Input  | Reset, active low      |
| F2  | EPAD        | Ground | Thermal and ground pad |

The pad list above is representative and is provided so that a module designer can estimate the interface early. The binding pin assignment is the manufacturer's package drawing for the exact variant ordered.

## 16. Reliability and Environmental

| Test                            | Condition                    | Result / Specification |
|---------------------------------|------------------------------|------------------------|
| Operating temperature           | -30 to +85 deg C             | (*) module dependent   |
| Storage temperature             | -40 to +125 deg C            | (*)                    |
| Temperature cycling             | -40 to +85 deg C, 500 cycles | JESD22-A104 (*)        |
| High-temperature operating life | 125 deg C, 1000 h            | JESD22-A108 (*)        |
| Humidity                        | 85 deg C / 85 % RH, 1000 h   | JESD22-A101 (*)        |
| ESD, HBM                        | 2000 V                       | JS-001 (*)             |
| ESD, CDM                        | 500 V                        | JS-002 (*)             |
| Moisture sensitivity level      | MSL 3                        | J-STD-020 (*)          |
| Vibration / drop                | Per module specification     | (*)                    |

## 17. Design and Integration Notes

### 17.1 Optical Matching

The chief ray angle at the image corner is approximately 20 degrees, so the lens must have a matching CRA curve. A lens with a much lower CRA produces colour shading and corner brightness falloff; a much higher CRA produces crosstalk and resolution loss at the corners. Always request the lens CRA curve from the lens supplier and compare it with the sensor CRA before committing to a module design. The lens image circle must cover the 6.51 mm diagonal with margin for the IR-cut filter holder.

For daylight colour rendering an IR-cut filter is required. Removing it makes the module NIR sensitive for day and night operation, but it shifts the white balance dramatically and requires a different colour matrix. State clearly in the listing whether the module is fixed IR-cut or IR-cut removable (ICR).

## 17.2 Power Supply and Decoupling

Place a 100 nF capacitor close to every supply pin and a bulk capacitor of 1 to 10  $\mu$ F per rail near the connector. AVDD must be quiet: a noisy 2.8 V rail shows up directly as horizontal banding in the image. Do not share the analog rail with switching loads such as an LED driver or a motor. If the host provides only 3.3 V, use a low-noise LDO rather than a switching regulator for AVDD.

## 17.3 Thermal Considerations

The die runs warm in continuous full-resolution mode. Provide a thermal path from the ground and thermal pad to the module substrate, and keep the sensor away from the SoC and the LED illuminator. Dark current roughly doubles every 6 to 8 degrees C, so a hot module shows more dark noise and more visible hot pixels. Within the rated range this is normal behaviour and not a manufacturing defect; explain it in the FAQ rather than treating it as a warranty case.

## 17.4 EMI and PCB Layout

Route the MIPI differential pairs with 100 Ohm differential impedance, equal length and matched intra-pair skew. Keep them away from the clock and from switching regulators, and reference them to a solid ground plane. Keep the MCLK trace short and guarded. Do not route high-speed traces under the sensor optical area.

**System-level rule: more than half of the issues reported by module makers as sensor problems turn out to be lens CRA mismatch, a noisy AVDD rail, or a poor MIPI layout. Check those three before opening a quality claim.**

## 18. Data Verification Note

Every value marked with an asterisk (\*) in this document is a typical reference figure, a placeholder, or a value that depends on the final package, the module and the test setup. Before this datasheet is published to customers or used in a product listing, each marked value must be replaced with the measured value for the actual product, or confirmed against the manufacturer's official datasheet.

| Category       | Examples of values to confirm                              |
|----------------|------------------------------------------------------------|
| Identification | Brand, model, SKU, country of origin                       |
| Optical        | Full well, SNR, dynamic range, QE, dark current, CRA       |
| Interface      | Lane rate, register addresses, I2C address                 |
| Electrical     | Typical and peak currents, standby current                 |
| Mechanical     | Package dimensions, pad count, optical centre              |
| Reliability    | ESD levels, MSL, temperature cycling results, certificates |
| Commercial     | MOQ, lead time, warranty, certificates                     |

## 19. Ordering Information and Commercial Terms

| Item                   | Specification                                             |
|------------------------|-----------------------------------------------------------|
| Order code example     | IS-5280-CSP-5MP-RAW10                                     |
| Delivery form          | CSP in tray; bare die on wafer or in waffle pack (*)      |
| Minimum order quantity | [MOQ] pieces - confirm per variant (*)                    |
| Lead time              | [X] weeks for production; samples in [Y] days (*)         |
| Sample policy          | [policy] (*)                                              |
| OEM / ODM              | Sensor re-marking and custom OTP data on request (*)      |
| Warranty               | 12 months from shipment against manufacturing defects (*) |

| Item                | Specification                                                                                             |
|---------------------|-----------------------------------------------------------------------------------------------------------|
| Warranty exclusions | ESD damage, reflow beyond the recommended profile, mechanical stress and use outside the rated conditions |

## 20. FAQ

### Q1. What is the difference between BSI and FSI and why does it matter?

In a back-illuminated (BSI) sensor the wiring layers sit behind the photodiode, so light reaches the silicon without passing between metal tracks. Compared with a front-illuminated sensor of the same pixel size, this gives higher quantum efficiency, better low-light performance and less crosstalk at the corners.

### Q2. Why is my image dark or noisy in low light?

Check the three variables in order: exposure time, analog gain and lens aperture. A lens with an F-number of 2.4 or slower collects far less light than an F2.0 lens. Raising gain amplifies noise as well as signal, so prefer a longer exposure and a faster lens before increasing gain.

### Q3. Can I connect this sensor directly to a small MCU such as an ESP32 or STM32?

Not through MIPI. Those MCUs do not have a MIPI CSI-2 receiver. You need either a host with a native MIPI CSI-2 port, or a module that integrates an ISP and exposes a parallel or USB interface. Always confirm the host interface before ordering.

### Q4. Why does the picture look green or colour shifted?

Almost always the IR-cut filter: it is missing, wrong, or the white balance has not been calibrated for the light source. A module without an IR-cut filter renders foliage and skin tones with a strong green or magenta cast under daylight.

### Q5. The frame rate is lower than the table in this document. Why?

Check the configured lane count, the PLL settings and the exposure time, then check whether the host can actually consume the bandwidth. A long exposure in a dark scene caps the frame rate physically, no matter what the interface can carry.

### Q6. Why do white dots or hot pixels appear in the image?

Hot pixels come from dark current and become more visible as the sensor warms up. A small number is normal for a CMOS sensor of this class and is handled by the ISP defect correction. Only an abnormal count on a cool sensor indicates a real defect.

**Q7. Do I need a separate ISP?**

Yes, if you use the bare sensor: the output is raw Bayer data. Either the host SoC must contain an ISP, or you should buy a module variant that already integrates one. Raw output is not a finished image.

**Q8. Is the module IR-cut or IR-cut removable?**

This depends on the SKU, not on the sensor. Each variant must be listed separately with its filter type, because a customer buying an IR-cut module for night vision will otherwise return it.

**Q9. Which lens should I use?**

An M12 board lens with an F-number of 2.0 to 2.2, a CRA curve matched to the sensor, and an image circle that covers at least 6.6 mm. A mismatched CRA is the most common cause of colour shading at the corners.

**Q10. The sensor does not respond on I2C. What should I check?**

Confirm that XSHUTDOWN is released, that MCLK is running, that the I2C address is correct and that the pull-up resistors are present, typically 2.2 to 4.7 kOhm. A sensor with no clock will not acknowledge on the bus.

**Q11. Is this sensor automotive qualified?**

Not by default. An AEC-Q100 qualified grade is only available if it is specifically ordered and the corresponding qualification reports are supplied. Do not advertise automotive use for the standard grade.

**Q12. Can I advertise this as a 5 megapixel camera?**

Yes, for the genuine sensor: the active array is 2880 x 1808, which is 5.17 MP. Do not interpolate a lower-resolution sensor up to 5 MP and sell it as such; that is the single most common cause of platform penalties in this category.

## 21. Revision History

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| Rev | Date           | Change                                                                                            |
|-----|----------------|---------------------------------------------------------------------------------------------------|
| 1.0 | September 2026 | Initial release as a technical reference template. Populate with measured data before publishing. |

## 22. Disclaimer

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This document is a technical reference template. All typical values, placeholders and values marked with an asterisk (\*) are indicative only and must be confirmed against the actual product, the manufacturer's official datasheet or measured data from the production module. Specifications are subject to change without notice.

Nothing in this document constitutes a warranty of performance for any particular application. The buyer is responsible for validating the sensor, the lens, the power design and the thermal design in the final product, and for ensuring that the finished product complies with the regulations of the destination market.