



Stratix II Device Handbook, Volume 1



101 Innovation Drive
San Jose, CA 95134
www.altera.com

Copyright © 2011 Altera Corporation. All rights reserved. Altera, The Programmable Solutions Company, the stylized Altera logo, specific device designations, and all other words and logos that are identified as trademarks and/or service marks are, unless noted otherwise, the trademarks and service marks of Altera Corporation in the U.S. and other countries. All other product or service names are the property of their respective holders. All Altera products are protected under numerous U.S. and foreign patents and pending applications, trademark rights, and copyrights. Altera warrants performance of its semiconductor products to conform specifications in accordance with Altera's standard warranty, but reserves the right to make

changes to any products and services at any time without notice. Altera assumes no responsibility or liability for any errors or for any damages arising out of the application or use of any information, product, or service described herein except as expressly agreed to in writing by Altera Corporation. Altera customers are advised to obtain the latest version of device specifications before relying on any published information and before placing orders for products or services.



U.S. EN 280-0001

Chapter Revision Dates	vii
-------------------------------------	------------

About this Handbook	i
How to Contact Altera	i
Typographic Conventions	i

Section I. Stratix II Device Family Data Sheet

Revision History	Section I-1
------------------------	-------------

Chapter 1. Introduction

Introduction	1-1
Features	1-1
Document Revision History	1-6

Chapter 2. Stratix II Architecture

Functional Description	2-1
Logic Array Blocks	2-3
LAB Interconnects	2-4
LAB Control Signals	2-5
Adaptive Logic Modules	2-6
ALM Operating Modes	2-9
Register Chain	2-20
Clear & Preset Logic Control	2-22
MultiTrack Interconnect	2-22
TriMatrix Memory	2-28
Memory Block Size	2-29
Digital Signal Processing Block	2-40
Modes of Operation	2-44
DSP Block Interface	2-44
PLLs & Clock Networks	2-48
Global & Hierarchical Clocking	2-48
Enhanced & Fast PLLs	2-57
Enhanced PLLs	2-68
Fast PLLs	2-69
I/O Structure	2-69
Double Data Rate I/O Pins	2-77
External RAM Interfacing	2-81
Programmable Drive Strength	2-83

Open-Drain Output	2-84
Bus Hold	2-84
Programmable Pull-Up Resistor	2-85
Advanced I/O Standard Support	2-85
On-Chip Termination	2-89
MultiVolt I/O Interface	2-93
High-Speed Differential I/O with DPA Support	2-96
Dedicated Circuitry with DPA Support	2-100
Fast PLL & Channel Layout	2-102
Document Revision History	2-104

Chapter 3. Configuration & Testing

IEEE Std. 1149.1 JTAG Boundary-Scan Support	3-1
SignalTap II Embedded Logic Analyzer	3-4
Configuration	3-4
Operating Modes	3-5
Configuration Schemes	3-7
Configuring Stratix II FPGAs with JRunner	3-10
Programming Serial Configuration Devices with SRunner	3-10
Configuring Stratix II FPGAs with the MicroBlaster Driver	3-11
PLL Reconfiguration	3-11
Temperature Sensing Diode (TSD)	3-11
Automated Single Event Upset (SEU) Detection	3-13
Custom-Built Circuitry	3-14
Software Interface	3-14
Document Revision History	3-14

Chapter 4. Hot Socketing & Power-On Reset

Stratix II	
Hot-Socketing Specifications	4-1
Devices Can Be Driven Before Power-Up	4-2
I/O Pins Remain Tri-Stated During Power-Up	4-2
Signal Pins Do Not Drive the V_{CCIO} , V_{CCINT} or V_{CCDD} Power Supplies	4-2
Hot Socketing Feature Implementation in Stratix II Devices	4-3
Power-On Reset Circuitry	4-5
Document Revision History	4-6

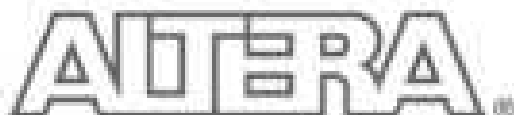
Chapter 5. DC & Switching Characteristics

Operating Conditions	5-1
Absolute Maximum Ratings	5-1
Recommended Operating Conditions	5-2
DC Electrical Characteristics	5-3
I/O Standard Specifications	5-4
Bus Hold Specifications	5-17
On-Chip Termination Specifications	5-17
Pin Capacitance	5-19
Power Consumption	5-20

Timing Model	5-20
Preliminary & Final Timing	5-20
I/O Timing Measurement Methodology	5-21
Performance	5-23
Internal Timing Parameters	5-34
Stratix II Clock Timing Parameters	5-41
Clock Network Skew Adders	5-50
IOE Programmable Delay	5-51
Default Capacitive Loading of Different I/O Standards	5-52
I/O Delays	5-54
Maximum Input & Output Clock Toggle Rate	5-66
Duty Cycle Distortion	5-77
DCD Measurement Techniques	5-78
High-Speed I/O Specifications	5-85
PLL Timing Specifications	5-91
External Memory Interface Specifications	5-94
ITAG Timing Specifications	5-96
Document Revision History	5-97

Chapter 6. Reference & Ordering Information

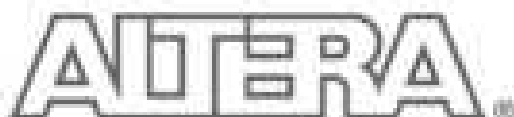
Software	7-1
Device Pin-Outs	7-1
Ordering Information	7-1
Document Revision History	7-1



Chapter Revision Dates

The chapters in this book, *Stratix II Device Handbook, Volume 1*, were revised on the following dates. Where chapters or groups of chapters are available separately, part numbers are listed.

Chapter 1.	Introduction
Revised:	May 2007
Part number:	5U51001-4.2
Chapter 2.	Stratix II Architecture
Revised:	May 2007
Part number:	5U51002-4.3
Chapter 3.	Configuration & Testing
Revised:	May 2007
Part number:	5U51003-4.2
Chapter 4.	Hot Socketing & Power-On Reset
Revised:	May 2007
Part number:	5U51004-3.2
Chapter 5.	DC & Switching Characteristics
Revised:	April 2011
Part number:	5U51005-4.3
Chapter 6.	Reference & Ordering Information
Revised:	April 2011
Part number:	5U51006-2.2



About this Handbook

This handbook provides comprehensive information about the Altera® Stratix® II family of devices.

How to Contact Altera

For the most up-to-date information about Altera products, refer to the following table.

Contact (1)	Contact Method	Address
Technical support	Website	www.altera.com/support
Technical training	Website	www.altera.com/training
	Email	custtran@altera.com
Product literature	Email	www.altera.com/literature
Altera literature services	Website	literature@altera.com
Non-technical support (General) (Software Licensing)	Email	nacomp@altera.com
	Email	authorization@altera.com

Note to table:

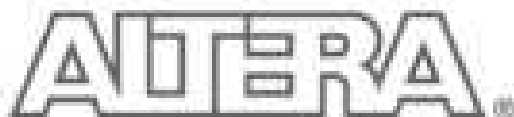
(1) You can also contact your local Altera sales office or sales representative.

Typographic Conventions

This document uses the typographic conventions shown below:

Visual Cue	Meaning
Bold Type with Initial Capital Letters	Command names, dialog box titles, checkbox options, and dialog box options are shown in bold, initial capital letters. Example: Save As dialog box.
bold type	External string parameters, directory names, project names, disk drive names, filenames, filename extensions, and software utility names are shown in bold type. Examples: f_max , iqdesigns directory, d: drive, chiptrip.gdf file.
<i>Italic Type with Initial Capital Letters</i>	Document titles are shown in italic type with initial capital letters. Example: <i>AN 75: High-Speed Board Design</i> .

Visual Cue	Meaning
<i>italic type</i>	Internal timing parameters and variables are shown in italic type. Examples: t_{rise} , $n + 1$. Variable names are enclosed in angle brackets (< >) and shown in italic type. Example: <file name>, <project name>.pdf file.
Initial Capital Letters	Keyboard keys and menu names are shown with initial capital letters. Examples: Delete key, the Options menu.
"Subheading Title"	References to sections within a document and titles of on-line help topics are shown in quotation marks. Example: "Typographic Conventions."
Courier type	Signal and port names are shown in lowercase Courier type. Examples: data1, tdl, input. Active-low signals are denoted by suffix n, e.g., $\overline{\text{resetn}}$. Anything that must be typed exactly as it appears is shown in Courier type. For example: c:\qdesigns\tutorial\chiptrip.gdf. Also, sections of an actual file, such as a Report File, references to parts of files (e.g., the AHDL keyword SUBDESIGN), as well as logic function names (e.g., TSL) are shown in Courier.
1., 2., 3., and a., b., c., etc.	Numbered steps are used in a list of items when the sequence of the items is important, such as the steps listed in a procedure.
■ ■ ■	Bullets are used in a list of items when the sequence of the items is not important.
✓	The checkmark indicates a procedure that consists of one step only.
	The hand points to information that requires special attention.
	The caution indicates required information that needs special consideration and understanding and should be read prior to starting or continuing with the procedure or process.
	The warning indicates information that should be read prior to starting or continuing the procedure or processes.
↵	The angled arrow indicates you should press the Enter key.
	The feet direct you to more information on a particular topic.



Section I. Stratix II Device Family Data Sheet

This section provides the data sheet specifications for Stratix® II devices. This section contains feature definitions of the internal architecture, configuration and JTAG boundary-scan testing information, DC operating conditions, AC timing parameters, a reference to power consumption, and ordering information for Stratix II devices.

This section contains the following chapters:

- Chapter 1, Introduction
- Chapter 2, Stratix II Architecture
- Chapter 3, Configuration & Testing
- Chapter 4, Hot Socketing & Power-On Reset
- Chapter 5, DC & Switching Characteristics
- Chapter 6, Reference & Ordering Information

Revision History

Refer to each chapter for its own specific revision history. For information on when each chapter was updated, refer to the Chapter Revision Dates section, which appears in the full handbook.

Introduction

The Stratix® II FPGA family is based on a 1.2-V, 90-nm, all-layer copper SRAM process and features a new logic structure that maximizes performance, and enables device densities approaching 180,000 equivalent logic elements (LEs). Stratix II devices offer up to 9 Mbits of on-chip, TriMatrix™ memory for demanding, memory intensive applications and has up to 96 DSP blocks with up to 384 (18-bit × 18-bit) multipliers for efficient implementation of high performance filters and other DSP functions. Various high-speed external memory interfaces are supported, including double data rate (DDR) SDRAM and DDR2 SDRAM, RDRAM II, quad data rate (QDR) II SRAM, and single data rate (SDR) SDRAM. Stratix II devices support various I/O standards along with support for 1-gigabit per second (Gbps) source synchronous signaling with DPA circuitry. Stratix II devices offer a complete clock management solution with internal clock frequency of up to 550 MHz and up to 12 phase-locked loops (PLLs). Stratix II devices are also the industry's first FPGAs with the ability to decrypt a configuration bitstream using the Advanced Encryption Standard (AES) algorithm to protect designs.

Features

The Stratix II family offers the following features:

- 15,600 to 179,400 equivalent LEs; see Table 1-1
- New and innovative adaptive logic module (ALM), the basic building block of the Stratix II architecture, maximizes performance and resource usage efficiency
- Up to 9,383,040 RAM bits (1,172,880 bytes) available without reducing logic resources
- TriMatrix memory consisting of three RAM block sizes to implement true dual-port memory and first-in first-out (FIFO) buffers
- High-speed DSP blocks provide dedicated implementation of multipliers (at up to 450 MHz), multiply-accumulate functions, and finite impulse response (FIR) filters
- Up to 16 global clocks with 24 clocking resources per device region
- Clock control blocks support dynamic clock network enable/disable, which allows clock networks to power down to reduce power consumption in user mode
- Up to 12 PLLs (four enhanced PLLs and eight fast PLLs) per device provide spread spectrum, programmable bandwidth, clock switch-over, real-time PLL reconfiguration, and advanced multiplication and phase shifting

- Support for numerous single-ended and differential I/O standards
- High-speed differential I/O support with DPA circuitry for 1-Gbps performance
- Support for high-speed networking and communications bus standards including Parallel RapidIO, SPI-4 Phase 2 (POS-PHY Level 4), HyperTransport™ technology, and SFI-4
- Support for high-speed external memory, including DDR and DDR2 SDRAM, RLDRAM II, QDR II SRAM, and SDR SDRAM
- Support for multiple intellectual property megafunctions from Altera MegaCore® functions and Altera Megafunction Partners Program (AMPP®) megafunctions
- Support for design security using configuration bitstream encryption
- Support for remote configuration updates

Table 1-1. *Stratix II FPGA Family Features*

Feature	EP2S15	EP2S30	EP2S60	EP2S90	EP2S130	EP2S180
ALMs	6,240	13,352	24,176	36,384	53,016	71,760
Adaptive look-up tables (ALUTs) (1)	12,480	27,104	48,352	72,768	106,032	143,520
Equivalent LEs (2)	15,600	33,880	60,440	90,960	132,540	179,400
M512 RAM blocks	104	202	329	488	699	930
MAK RAM blocks	78	144	255	408	609	768
M-RAM blocks	0	1	2	4	6	9
Total RAM bits	419,328	1,369,728	2,544,192	4,520,488	6,747,840	9,363,040
DSP blocks	12	16	36	48	63	96
18-bit × 18-bit multipliers (3)	48	64	144	192	252	384
Enhanced PLLs	2	2	4	4	4	4
Fast PLLs	4	4	8	8	8	8
Maximum user I/O pins	366	500	718	902	1,126	1,170

Notes for Table 1-1:

- (1) One ALM contains two ALUTs. The ALUT is the cell used in the Quartus® II software for logic synthesis.
- (2) This is the equivalent number of LEs in a Stratix device (four-input LUT-based architecture).
- (3) These multipliers are implemented using the DSP blocks.

Stratix II devices are available in space-saving FineLine BGA® packages (see Tables 1-2 and 1-3).

Table 1-2. Stratix II Package Options & I/O Pin Counts *Notes (1), (2)*

Device	484-Pin FineLine BGA	484-Pin Hybrid FineLine BGA	672-Pin FineLine BGA	788-Pin FineLine BGA	1,020-Pin FineLine BGA	1,508-Pin FineLine BGA
EP2S15	342		306			
EP2S30	342		600			
EP2S60 (3)	334		492		718	
EP2S90 (3)		308		534	758	902
EP2S130 (3)				534	742	1,126
EP2S180 (3)					742	1,170

Notes to Table 1-2:

- (1) All I/O pin counts include eight dedicated clock input pins (`clk0p`, `clk1a`, `clk0p`, `clk0n`, `clk1p`, `clk1n`, `clk2p`, and `clk2n`) that can be used for data inputs.
- (2) The Quartus II software I/O pin counts include one additional pin, `PLL_ENA`, which is not available as general-purpose I/O pins. The `PLL_ENA` pin can only be used to enable the PLLs within the device.
- (3) The I/O pin counts for the EP2S90, EP2S90, EP2S130, and EP2S180 devices in the 1020-pin and 1508-pin packages include eight dedicated fast PLL clock inputs (`FPLL0CLKp/n`, `FPLL0CLKp/n`, `FPLL0CLKp/n`, and `FPLL1CLKp/n`) that can be used for data inputs.

Table 1-3. Stratix II FineLine BGA Package Sizes

Dimension	484 Pin	484-Pin Hybrid	672 Pin	788 Pin	1,020 Pin	1,508 Pin
Pitch (mm)	1.00	1.00	1.00	1.00	1.00	1.00
Area (mm ²)	529	729	729	641	1,069	1,600
Length × width (mm × mm)	23 × 23	27 × 27	27 × 27	29 × 29	33 × 33	40 × 40

All Stratix II devices support vertical migration within the same package (for example, you can migrate between the EP2S15, EP2S30, and EP2S60 devices in the 672-pin FineLine BGA package). Vertical migration means that you can migrate to devices whose dedicated pins, configuration pins, and power pins are the same for a given package across device densities.

To ensure that a board layout supports migratable densities within one package offering, enable the applicable vertical migration path within the Quartus II software (Assignments menu > Device > Migration Devices).

After compilation, check the information messages for a full list of I/O, DQ, LVDS, and other pins that are not available because of the selected migration path.

Table 1-4 lists the Stratix II device package offerings and shows the total number of non-migratable user I/O pins when migrating from one density device to a larger density device. Additional I/O pins may not be migratable if migrating from the larger device to the smaller density device.

 When moving from one density to a larger density, the larger density device may have fewer user I/O pins. The larger device requires more power and ground pins to support the additional logic within the device. Use the Quartus II Pin Planner to determine which user I/O pins are migratable between the two devices.

Table 1-4. Total Number of Non-Migratable I/O Pins for Stratix II Vertical Migration Paths

Vertical Migration Path	484-Pin FineLine BGA	672-Pin FineLine BGA	780-Pin FineLine BGA	1028-Pin FineLine BGA	1508-Pin FineLine BGA
EP2S15 to EP2S30	0 (1)	0			
EP2S15 to EP2S60	8 (1)	0			
EP2S30 to EP2S60	8 (1)	8			
EP2S60 to EP2S90				0	
EP2S60 to EP2S130				0	
EP2S60 to EP2S180				0	
EP2S90 to EP2S130			0 (1)	16	17
EP2S90 to EP2S180				16	0
EP2S130 to EP2S180				0	0

Note for Table 1-4:

(1) Some of the DQ/DQS pins are not migratable. Refer to the Quartus II software information messages for more detailed information.

 To determine if your user I/O assignments are correct, run the I/O Assignment Analysis command in the Quartus II software (Processing > Start > Start I/O Assignment Analysis).



Refer to the *I/O Management* chapter in volume 2 of the *Quartus II Handbook* for more information on pin migration.

Stratix II devices are available in up to three speed grades, -3, -4, and -5, with -3 being the fastest. Table 1-5 shows Stratix II device speed-grade offerings.

Table 1-5. Stratix II Device Speed Grades

Device	Temperature Grade	484-Pin FineLine BGA	484-Pin Hybrid FineLine BGA	872-Pin FineLine BGA	780-Pin FineLine BGA	1,020-Pin FineLine BGA	1,508-Pin FineLine BGA
EP2S15	Commercial	-3, -4, -5		-3, -4, -5			
	Industrial	-4		-4			
EP2S30	Commercial	-3, -4, -5		-3, -4, -5			
	Industrial	-4		-4			
EP2S60	Commercial	-3, -4, -5		-3, -4, -5		-3, -4, -5	
	Industrial	-4		-4		-4	
EP2S90	Commercial		-4, -5		-4, -5	-3, -4, -5	-3, -4, -5
	Industrial					-4	-4
EP2S130	Commercial				-4, -5	-3, -4, -5	-3, -4, -5
	Industrial					-4	-4
EP2S180	Commercial					-3, -4, -5	-3, -4, -5
	Industrial					-4	-4

Document Revision History

Table 1-6 shows the revision history for this chapter.

<i>Table 1-6. Document Revision History</i>		
Date and Document Version	Changes Made	Summary of Changes
May 2007, v4.2	Moved Document Revision History to the end of the chapter.	—
April 2006, v4.1	• Updated "Features" section. • Removed Note 4 from Table 1-2. • Updated Table 1-4.	—
December 2005, v4.0	• Updated Tables 1-2, 1-4, and 1-5. • Updated Figure 2-43.	—
July 2005, v3.1	• Added vertical migration information, including Table 1-4. • Updated Table 1-5.	—
May 2005, v3.0	• Updated "Features" section. • Updated Table 1-2.	—
March 2005, v2.1	Updated "Introduction" and "Features" sections.	—
January 2005, v2.0	Added note to Table 1-2.	—
October 2004, v1.2	Updated Tables 1-2, 1-3, and 1-5.	—
July 2004, v1.1	• Updated Tables 1-1 and 1-2. • Updated "Features" section.	—
February 2004, v1.0	Added document to the Stratix II Device Handbook.	—

Functional Description

Stratix® II devices contain a two-dimensional row- and column-based architecture to implement custom logic. A series of column and row interconnects of varying length and speed provides signal interconnects between logic array blocks (LABs), memory block structures (M512 RAM, M4K RAM, and M-RAM blocks), and digital signal processing (DSP) blocks.

Each LAB consists of eight adaptive logic modules (ALMs). An ALM is the Stratix II device family's basic building block of logic providing efficient implementation of user logic functions. LABs are grouped into rows and columns across the device.

M512 RAM blocks are simple dual-port memory blocks with 512 bits plus parity (576 bits). These blocks provide dedicated simple dual-port or single-port memory up to 18-bits wide at up to 300 MHz. M512 blocks are grouped into columns across the device in between certain LABs.

M4K RAM blocks are true dual-port memory blocks with 4K bits plus parity (4,608 bits). These blocks provide dedicated true dual-port, simple dual-port, or single-port memory up to 36-bits wide at up to 350 MHz. These blocks are grouped into columns across the device in between certain LABs.

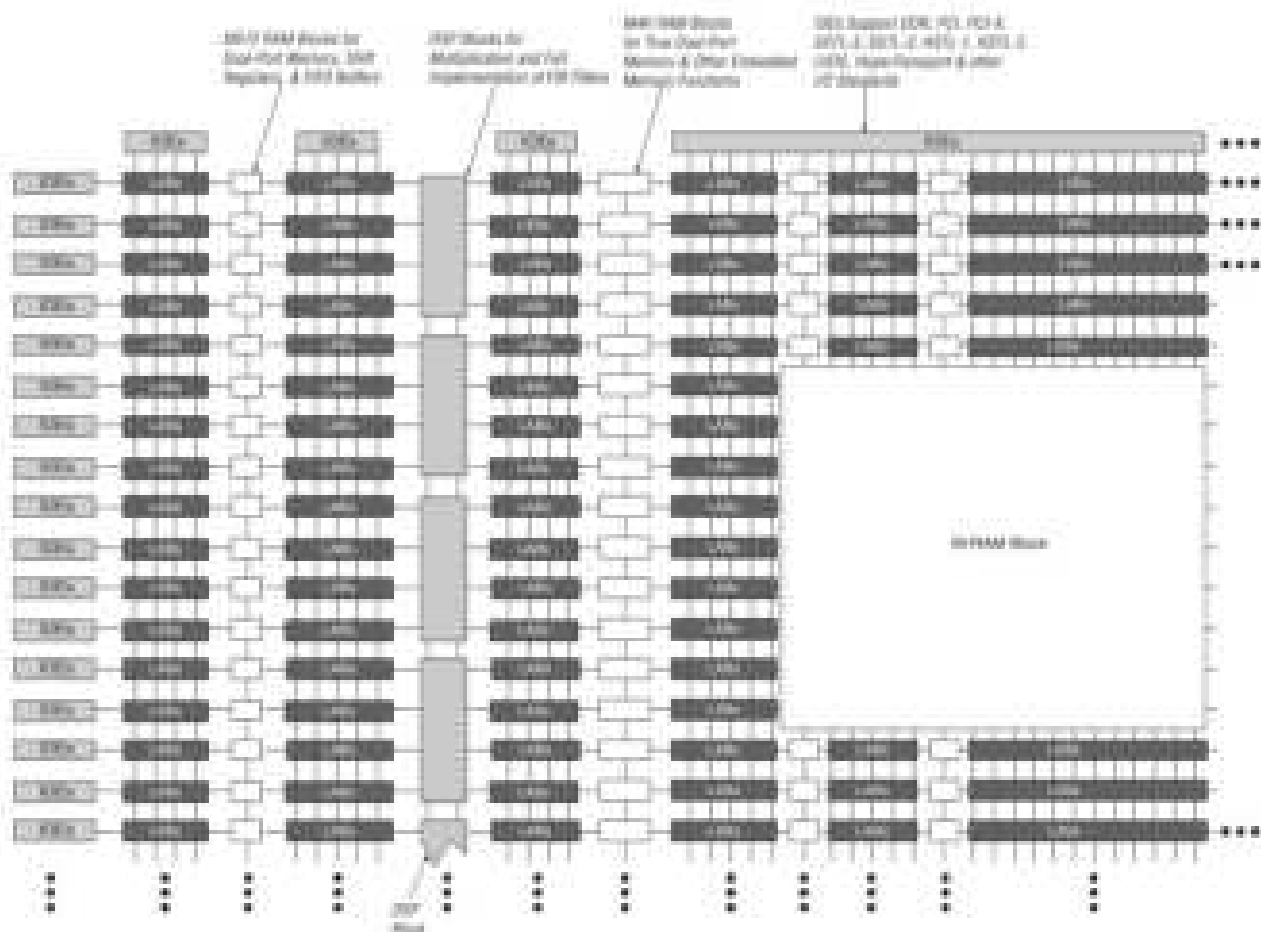
M-RAM blocks are true dual-port memory blocks with 512K bits plus parity (589,824 bits). These blocks provide dedicated true dual-port, simple dual-port, or single-port memory up to 144-bits wide at up to 420 MHz. Several M-RAM blocks are located individually in the device's logic array.

DSP blocks can implement up to either eight full-precision 9×9 -bit multipliers, four full-precision 18×18 -bit multipliers, or one full-precision 36×36 -bit multiplier with add or subtract features. The DSP blocks support Q1.15 format rounding and saturation in the multiplier and accumulator stages. These blocks also contain shift registers for digital signal processing applications, including finite impulse response (FIR) and infinite impulse response (IIR) filters. DSP blocks are grouped into columns across the device and operate at up to 450 MHz.

Each Stratix II device I/O pin is fed by an I/O element (IOE) located at the end of LAB rows and columns around the periphery of the device. I/O pins support numerous single-ended and differential I/O standards. Each IOE contains a bidirectional I/O buffer and six registers for registering input, output, and output-enable signals. When used with dedicated clocks, these registers provide exceptional performance and interface support with external memory devices such as DDR and DDR2 SDRAM, RDRAM II, and QDR II SRAM devices. High-speed serial interface channels with dynamic phase alignment (DPA) support data transfer at up to 1 Gbps using LVDS or HyperTransport™ technology I/O standards.

Figure 2-1 shows an overview of the Strato II device.

Figure 2-1. Stratix II Block Diagram



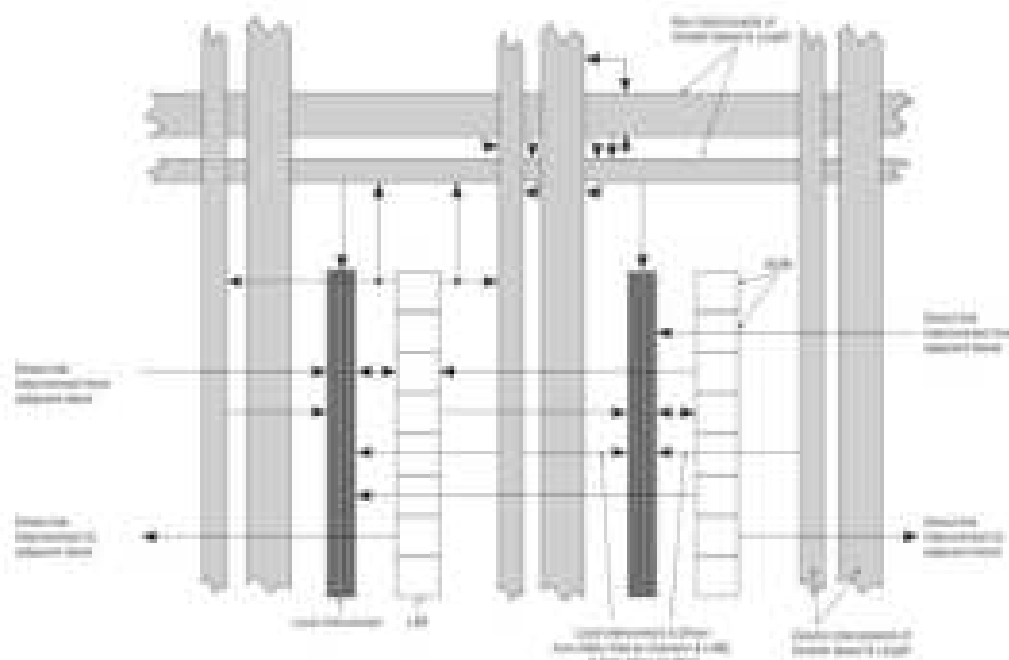
The number of M512 RAM, M4K RAM, and DSP blocks varies by device along with row and column numbers and M-RAM blocks. Table 2-1 lists the resources available in Stratix II devices.

Table 2-1. Stratix II Device Resources

Device	M512 RAM Columns/Blocks	M4K RAM Columns/Blocks	M-RAM Blocks	DSP Block Columns/Blocks	LAB Columns	LAB Rows
EP2S15	4 / 104	3 / 78	0	2 / 12	30	26
EP2S30	6 / 202	4 / 144	1	2 / 16	48	38
EP2S60	7 / 329	5 / 255	2	3 / 36	62	51
EP2S60	8 / 488	6 / 408	4	3 / 48	71	68
EP2S130	9 / 699	7 / 609	6	3 / 63	81	67
EP2S180	11 / 930	8 / 768	9	4 / 96	100	96

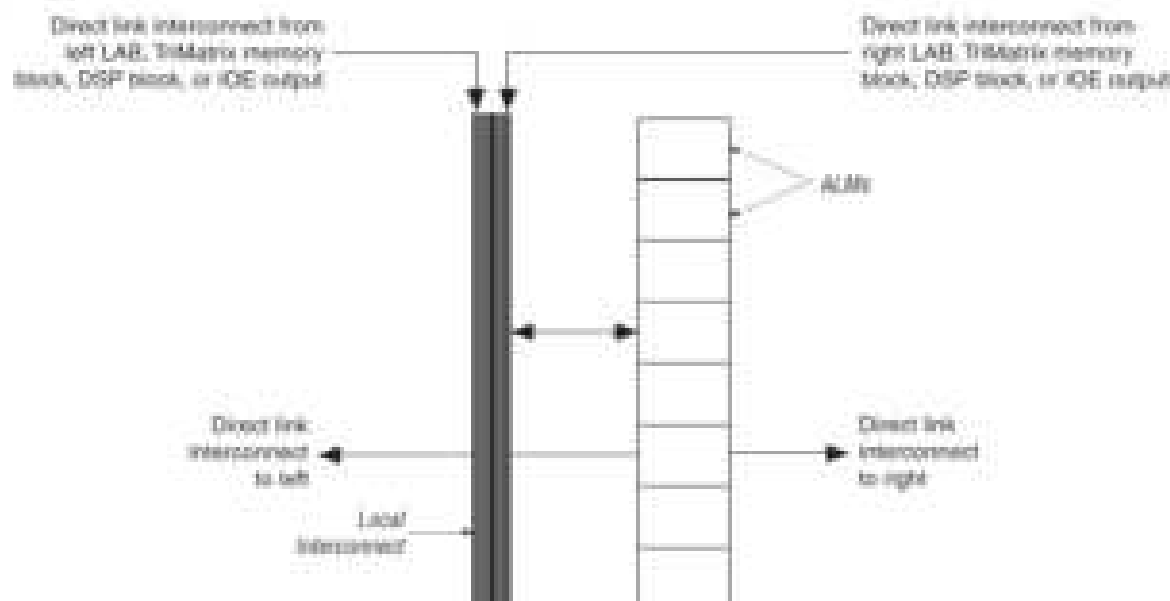
Logic Array Blocks

Each LAB consists of eight ALMs, carry chains, shared arithmetic chains, LAB control signals, local interconnect, and register chain connection lines. The local interconnect transfers signals between ALMs in the same LAB. Register chain connections transfer the output of an ALM register to the adjacent ALM register in an LAB. The Quartus® II Compiler places associated logic in an LAB or adjacent LABs, allowing the use of local, shared arithmetic chain, and register chain connections for performance and area efficiency. Figure 2-2 shows the Stratix II LAB structure.

Figure 2-2. Stratix II LAB Structure

LAB Interconnects

The LAB local interconnect can drive ALMs in the same LAB. It is driven by column and row interconnects and ALM outputs in the same LAB. Neighboring LABs, M512 RAM blocks, M4K RAM blocks, M-RAM blocks, or DSP blocks from the left and right can also drive an LAB's local interconnect through the direct link connection. The direct link connection feature minimizes the use of row and column interconnects, providing higher performance and flexibility. Each ALM can drive 24 ALMs through fast local and direct link interconnects. Figure 2-3 shows the direct link connection.

Figure 2-3. Direct Link Connection

LAB Control Signals

Each LAB contains dedicated logic for driving control signals to its ALMs. The control signals include three clocks, three clock enables, two asynchronous clears, synchronous clear, asynchronous preset/load, and synchronous load control signals. This gives a maximum of 11 control signals at a time. Although synchronous load and clear signals are generally used when implementing counters, they can also be used with other functions.

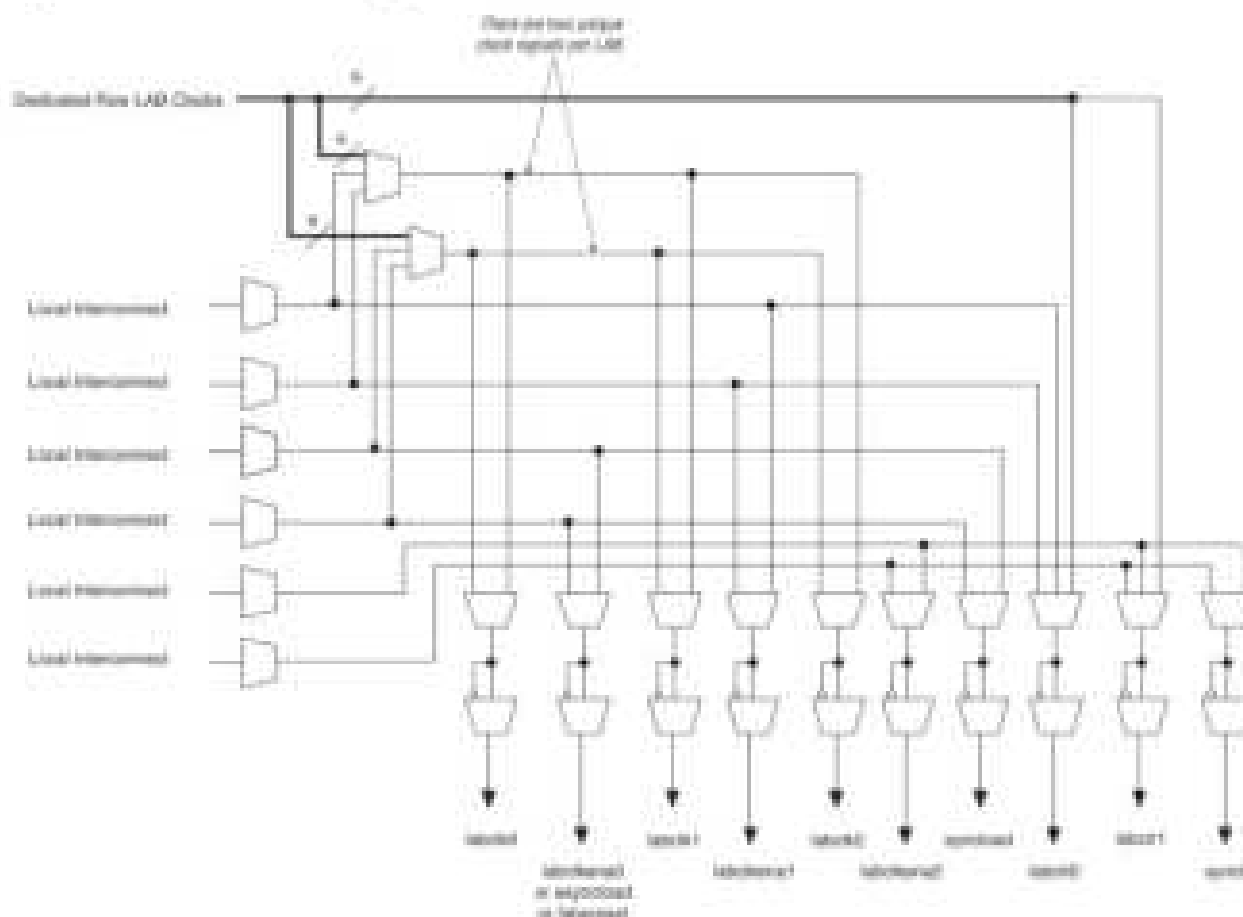
Each LAB can use three clocks and three clock enable signals. However, there can only be up to two unique clocks per LAB, as shown in the LAB control signal generation circuit in Figure 2-4. Each LAB's clock and clock enable signals are linked. For example, any ALM in a particular LAB using the `Label1k1` signal also uses `Label1kema1`. If the LAB uses both the rising and falling edges of a clock, it also uses two LAB-wide clock signals. De-asserting the clock enable signal turns off the corresponding LAB-wide clock.

Each LAB can use two asynchronous clear signals and an asynchronous load/preset signal. By default, the Quartus II software uses a NOT gate push-back technique to achieve preset. If you disable the NOT gate push-up option or assign a given register to power up high using the Quartus II software, the preset is achieved using the asynchronous load

signal with asynchronous load data input tied high. When the asynchronous load/preset signal is used, the `labc1kena0` signal is no longer available.

The LAB row clocks [5...0] and LAB local interconnect generate the LAB-wide control signals. The MultiTrack™ interconnect's inherent low skew allows clock and control signal distribution in addition to data. Figure 2-4 shows the LAB control signal generation circuit.

Figure 2-4. LAB-Wide Control Signals



Adaptive Logic Modules

The basic building block of logic in the Stratix II architecture, the adaptive logic module (ALM), provides advanced features with efficient logic utilization. Each ALM contains a variety of look-up table (LUT)-based resources that can be divided between two adaptive LUTs (ALUTs). With up to eight inputs to the two ALUTs, one ALM can implement various combinations of two functions. This adaptability allows the ALM to be

completely backward-compatible with four-input LUT architectures. One ALM can also implement any function of up to six inputs and certain seven-input functions.

In addition to the adaptive LUT-based resources, each ALM contains two programmable registers, two dedicated full adders, a carry chain, a shared arithmetic chain, and a register chain. Through these dedicated resources, the ALM can efficiently implement various arithmetic functions and shift registers. Each ALM drives all types of interconnects: local, row, column, carry chain, shared arithmetic chain, register chain, and direct link interconnects. Figure 2-5 shows a high-level block diagram of the Stratus II ALM while Figure 2-6 shows a detailed view of all the connections in the ALM.

Figure 2-5. High-Level Block Diagram of the Stratix II ALM

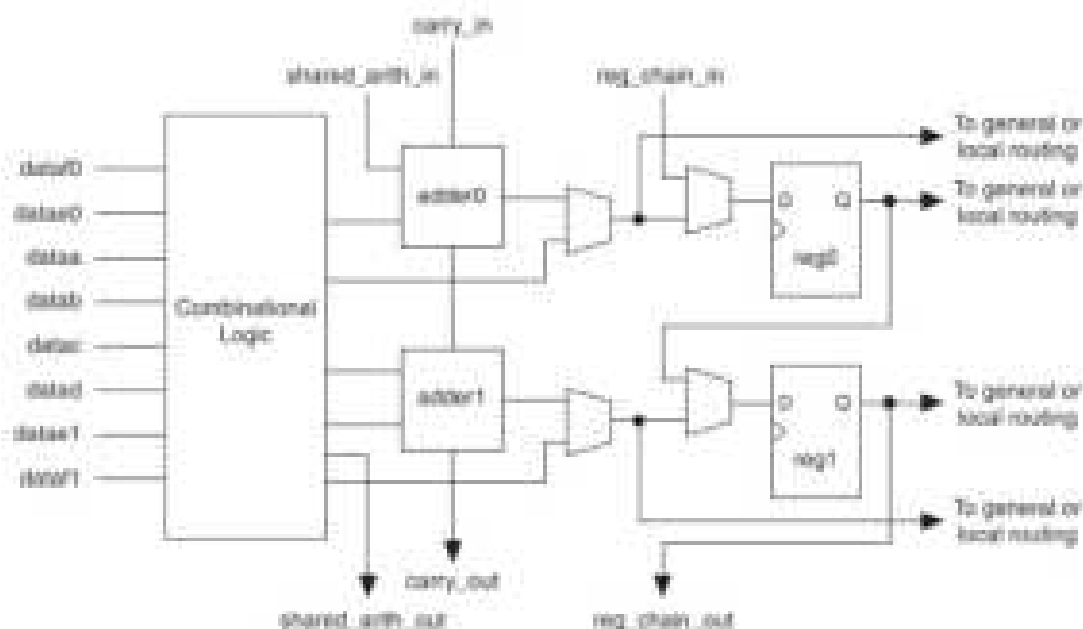
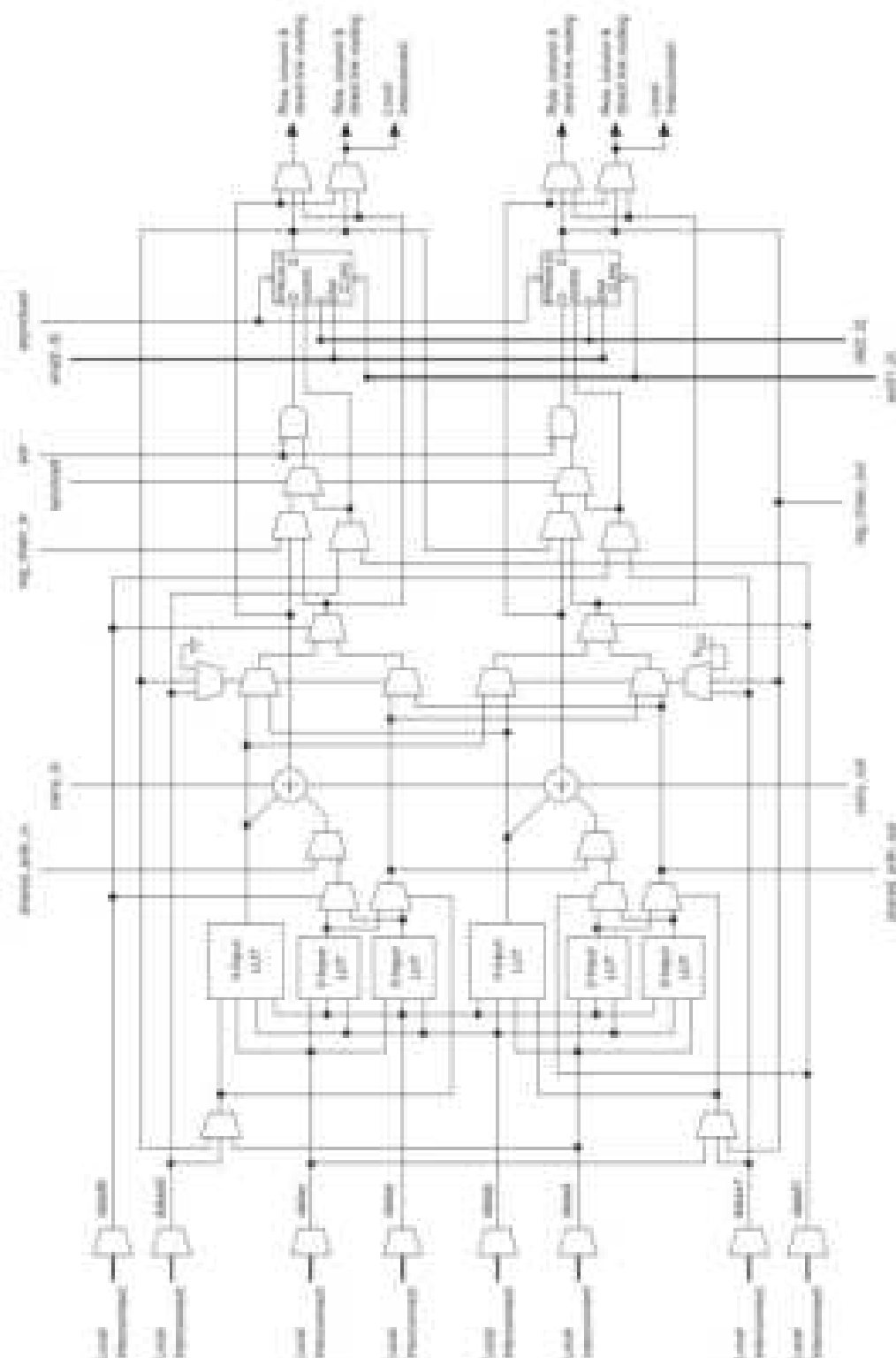


Figure 2-6. Stratix II ALM Details



One ALM contains two programmable registers. Each register has data, clock, clock enable, synchronous and asynchronous clear, asynchronous load data, and synchronous and asynchronous load/preset inputs. Global signals, general-purpose I/O pins, or any internal logic can drive the register's clock and clear control signals. Either general-purpose I/O pins or internal logic can drive the clock enable, preset, asynchronous load, and asynchronous load data. The asynchronous load data input comes from the `data.se` or `data.af` input of the ALM, which are the same inputs that can be used for register packing. For combinational functions, the register is bypassed and the output of the LUT drives directly to the outputs of the ALM.

Each ALM has two sets of outputs that drive the local, row, and column routing resources. The LUT, adder, or register output can drive these output drivers independently (see Figure 2-6). For each set of output drivers, two ALM outputs can drive column, row, or direct link routing connections, and one of these ALM outputs can also drive local interconnect resources. This allows the LUT or adder to drive one output while the register drives another output. This feature, called register packing, improves device utilization because the device can use the register and the combinational logic for unrelated functions. Another special packing mode allows the register output to feed back into the LUT of the same ALM so that the register is packed with its own fan-out LUT. This provides another mechanism for improved fitting. The ALM can also drive out registered and unregistered versions of the LUT or adder output.



See the *Performance & Logic Efficiency Analysis of Stratix II Devices White Paper* for more information on the efficiencies of the Stratix II ALM and comparisons with previous architectures.

ALM Operating Modes

The Stratix II ALM can operate in one of the following modes:

- Normal mode
- Extended LUT mode
- Arithmetic mode
- Shared arithmetic mode

Each mode uses ALM resources differently. In each mode, eleven available inputs to the ALM—the eight data inputs from the LAB local interconnect; `carry-in` from the previous ALM or LAB; the shared arithmetic chain connection from the previous ALM or LAB; and the register chain connection—are directed to different destinations to implement the desired logic function. LAB-wide signals provide clock, asynchronous clear, asynchronous preset/load, synchronous clear,

synchronous load, and clock enable control for the register. These LAB-wide signals are available in all ALM modes. See the "LAB Control Signals" section for more information on the LAB-wide control signals.

The Quartus II software and supported third-party synthesis tools, in conjunction with parameterized functions such as library of parameterized modules (LPM) functions, automatically choose the appropriate mode for common functions such as counters, adders, subtractors, and arithmetic functions. If required, you can also create special-purpose functions that specify which ALM operating mode to use for optimal performance.

Normal Mode

The normal mode is suitable for general logic applications and combinational functions. In this mode, up to eight data inputs from the LAB local interconnect are inputs to the combinational logic. The normal mode allows two functions to be implemented in one Stratix II ALM, or an ALM to implement a single function of up to six inputs. The ALM can support certain combinations of completely independent functions and various combinations of functions which have common inputs.

Figure 2-7 shows the supported LUT combinations in normal mode.