

PRODUCT SPECIFICATION

TFT LCD MODULE

MODEL : KWH028Q29-F01 Version: 1.0

【 】 Preliminary Specification

【 ◆ 】 Finally Specification

CUSTOMER'S APPROVAL	
SIGNATURE:	DATE:

- It signifies that you fully understand and accept all the contents of this specification if you sign and send back the first page of this specifications.

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Revision record

[illegible]

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1. General Description

1.1 Description

KWH028Q29-F01 is a Transmissive type color active matrix liquid crystal display (LCD), which uses amorphous thin film transistor (TFT) as switching devices. This product is composed of a TFT LCD panel, driver IC, FPC and backlight unit . The following table described the features of FORMIKE KWH028Q29-F01.

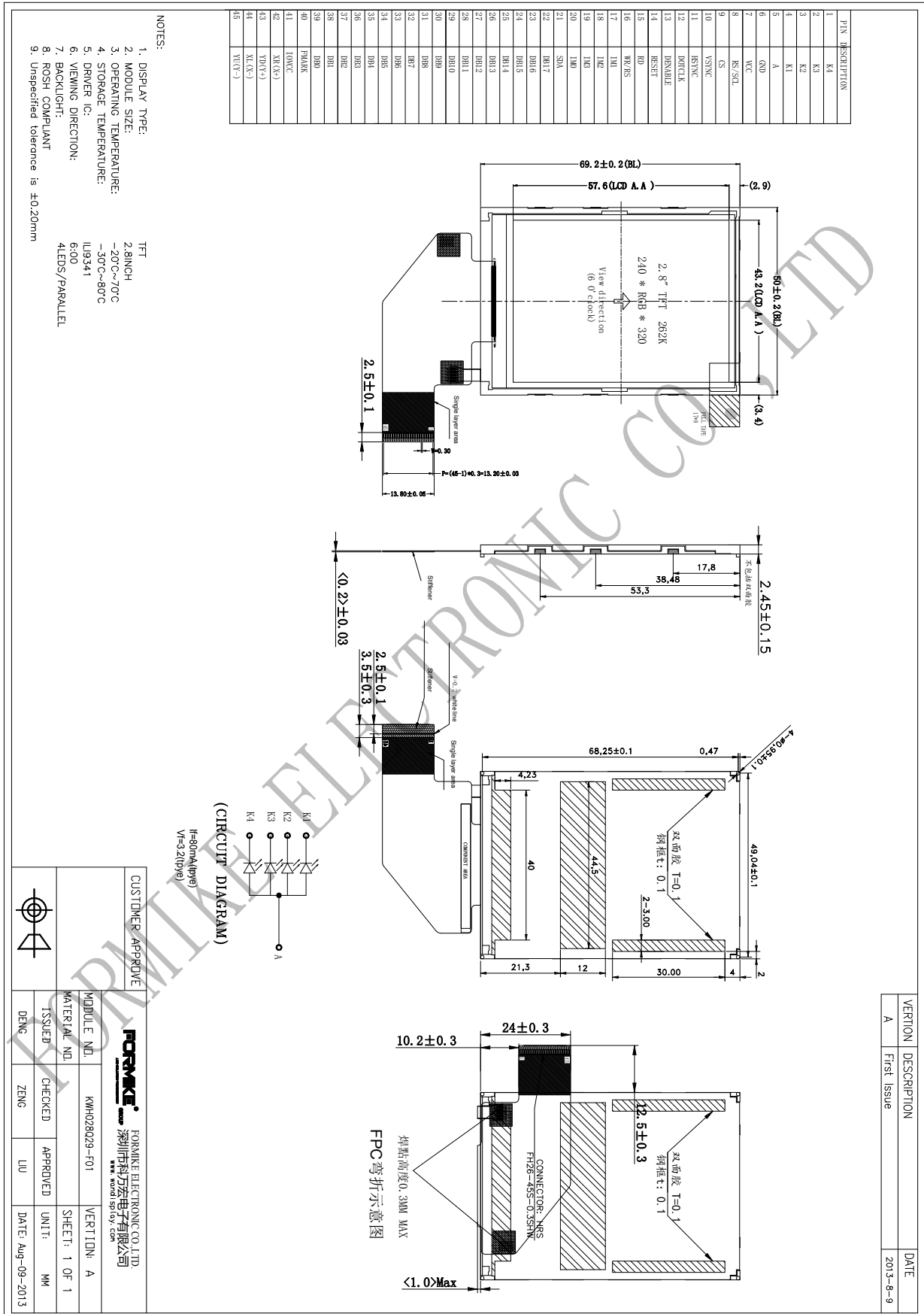
1.2 Application

Mobile phone, Multimedia products
and other electronic Products
Etc.

1.3 Features:

Features	Description	UNITS
LCD type	2.8" TFT	--
Dot arrangement	240 (RGB) × 320	dots
Driver IC	ILI9341	--
Color Depth	262K	
Interface	RGB ,MCU,Serial Interface	--
View Direction	6 O'clock	--
Module size	50.0(W) × 69.2 (H) × 2.45(T)	mm
Active area	43.2(W) × 57.6(H)	mm
Dot pitch	0.18 (W) × 0.18 (H)	mm
Back Light	4 White LED In parallel	--
With/Without TSP	Without TSP	
Weight(g)	TBD	

2. External Dimensions



3. Interface Description

PIN NO.	PIN NAME	DESCRIPTION
1-4	K4-K1	Power supply for LED backlight Cathode input
5	A	Power supply for LED backlight Anode input
6	GND	Ground.
7	VCC	Power supply (+2.3V~+3.3V).
8	RS/SCL	This pin is used to select "data or command" in the parallel interface or 4-wire 8-bit serial data interface. When RS="1", data is selected. When RS="0", command is selected. This pin is used serial interface clock in 3-wire 9-bit/4-wire 8-bit serial data interface. Fix to IOVCC or GND level when not in use.
9	CS	Chip select input pin(" low" enable).
10	VSYNC	Frame synchronizing signal for RGB interface operation. Fix to IOVCC or GND level when not in use.
11	HSYNC	Line synchronizing signal for RGB interface operation. Fix to IOVCC or GND level when not in use.
12	DOTCLK	Dot clock signal for RGB interface operation. Fix to IOVCC or GND level when not in use.
13	ENABLE	Data enable signal for RGB interface operation. Fix to IOVCC or GND level when not in use.
14	RESET	This signal will reset the device and must be applied to properly initialize the chip. Signal is active low.
15	RD	8080-I/8080-II system(RD):Serves as a read signal and MCU read data at the rising edge. Fix to IOVCC level when not in use.
16	WR/RS	8080-I/8080-II system(WR):Serves as a write signal and writes data at the rising edge. 4-Line system(RS):Serves as command or parameter select. Fix to IOVCC level when not in use.
17	IM1	The selection of the given interfaces are done by external IM[3:0] Pins and shown as below Note 1.
18	IM2	
19	IM3	
20	IM0	
21	SDA	The data is applied on the rising edge of the SCL signal. Fix to IOVCC or GND level when not in use.
22-39	DB17-DB0	18-Bit parallel data bus for MCU system and RGB interface mode. Fix to GND level when not in use.
40	FMARK	Frame Synchronous Signal. If not used, please open this pin.
41	IOVCC	Power supply Voltage for I/O Interface (1.65V/3.3V).
42	XR	Touch Panel Right Side Wire.
43	YD	Touch Panel Down Side Wire.
44	XL	Touch Panel Left Side Wire.
45	YU	Touch Panel Up Side Wire.

NOTE 1:

ILI9341 provides four kinds of MCU system interface with 8080-1 /8080-II series parallel interface and 3-/4-line serial interface. The selection of the given interfaces are done by external IM [3:0] pins and shown as below:

IM3	IM2	IM1	IM0	MCU-Interface Mode	Pins in use	
					Register/Command	GRAM
0	0	0	0	8080 MCU 8-bit bus interface - I	D[7:0]	D[7:0], WRX, RDX, CSX, D/CX
0	0	0	1	8080 MCU 16-bit bus interface - I	D[7:0]	D[15:0], WRX, RDX, CSX, D/CX
0	0	1	0	8080 MCU 8-bit bus interface - II	D[7:0]	D[8:0], WRX, RDX, CSX, D/CX
0	0	1	1	8080 MCU 16-bit bus interface - II	D[7:0]	D[17:0], WRX, RDX, CSX, D/CX
0	1	0	1	3-wire 9-bit data serial interface - I	SCL, SDA, CSX	
0	1	1	0	4-wire 8-bit data serial interface - I	SCL, SDA, D/CX, CSX	
1	0	0	0	8080 MCU 16-bit bus interface - III	D[8:1]	D[17:10], D[8:1], WRX, RDX, CSX, D/CX
1	0	0	1	8080 MCU 8-bit bus interface - III	D[17:10]	D[17:10], WRX, RDX, CSX, D/CX
1	0	1	0	8080 MCU 16-bit bus interface - III	D[8:1]	D[17:0], WRX, RDX, CSX, D/CX
1	0	1	1	8080 MCU 8-bit bus interface - III	D[17:10]	D[17:8], WRX, RDX, CSX, D/CX
1	1	0	1	3-wire 9-bit data serial interface - II	SCL, SDA, SDO, CSX	
1	1	1	0	4-wire 8-bit data serial interface - II	SCL, SDA, D/CX, SDO, CSX	

4. Absolute Maximum Ratings

The absolute maximum rating is listed on following table. When ILI9341 is used out of the absolute maximum ratings, ILI9341 may be permanently damaged. To use ILI9341 within the following electrical characteristic limitation is strongly recommended for normal operation. If these electrical characteristic conditions are exceeded during normal operation, ILI9341 will malfunction and cause poor reliability.

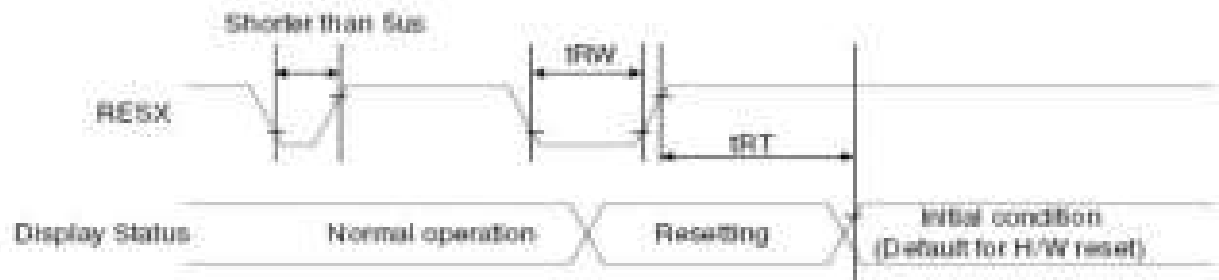
Item	Symbol	Unit	Value
Supply voltage	VCI	V	-0.3 ~ +4.6
Supply voltage (Logic)	VDDI	V	-0.3 ~ +4.6
Supply voltage (Digital)	VDORE	V	-0.3 ~ +2.0
Driver supply voltage	VGH-VGL	V	-0.3 ~ +32.0
Logic input voltage range	VIN	V	-0.3 ~ VDDI + 0.3
Logic output voltage range	VO	V	-0.3 ~ VDDI + 0.3
Operating temperature	T _{opr}	°C	-40 ~ +85
Storage temperature	T _{stg}	°C	-55 ~ +110
Note: If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.			

5. Electrical Characteristics

Item	Symbol	Unit	Condition	Min.	Typ.	Max.	Note
Power and Operation Voltage							
Analog Operating Voltage	VCI	V	Operating voltage	2.5	2.8	3.3	Note2
Logic Operating Voltage	VDDI	V	IO supply voltage	1.65	2.8	3.3	Note2
Digital Operating voltage	VCORE	V	Digital supply voltage	-	1.5	-	Note2
Gate Driver High Voltage	VGH	V	-	10.0	-	16.0	Note3
Gate Driver Low Voltage	VGL	V	-	-10.0	-	-5.0	Note3
Driver Supply Voltage	-	V	VGH-VGL	15	-	28	Note3
Current consumption during standby mode	I _{st}	μA	VCI=2.8V, T _a =25 °C	-	-	100	-
Input and Output							
Logic High Level Input Voltage	V _{IH}	V	-	0.7*VDDI	-	VDDI	Note1,2,3
Logic Low Level Input Voltage	V _{IL}	V	-	VSS	-	0.3*VDDI	Note1,2,3
Logic High Level Output Voltage	V _{OH}	V	I _{OL} ≤1.0mA	0.8*VDDI	-	VDDI	Note1,2,3
Logic Low Level Output Voltage	V _{OL}	V	I _{OL} ≤1.0mA	VSS	-	0.2*VDDI	Note1,2,3
Logic High Level Input Current	I _{IH}	μA	-	-	-	1	Note1,2,3
Logic Low Level Input Current	I _{IL}	μA	-	-1	-	-	Note1,2,3
Logic Input Leakage Current	I _{LEA}	μA	V _{IN} =VDDI or VSS	-0.1	-	+0.1	Note1,2,3
VCOM Operation							
VCOM High Voltage	VCOMH	V	C _{com} =12nF	2.5	-	5.0	Note3
VCOM Low Voltage	VCOML	V	C _{com} =12nF	-2.5	-	0.0	Note3
VCOM Amplitude Voltage	VCOMA	V	VCOMH-VCOML	4.0	-	5.5	Note3
Source Driver							
Source Output Range	V _{out}	V	-	0.1	-	DDVDH-0.1	Note4
Gamma Reference Voltage	GVDD	V	-	-3.0	-	5.0	Note3
Output Deviation Voltage (Source Output channel)	V _{dev}	mV	S _{out} ≤4.2V S _{out} ≤0.8V	-	-	20	Note4
Output Offset Voltage	V _{OFSET}	mV	4.2V>S _{out} ≤0.8V	-	-	15	-
			-	-	-	35	Note7
Booster Operation							
1 st Booster (VCIx2) Voltage	DDVDH	V	-	4.95 (Note 5)	-	5.8 (Note 6)	Note3
1 st Booster (VCIx2) Drop Voltage	VCIx2 drop	%	loading=1mA	-	-	5	Note3
Linear Range	V _{line}	V	-	0.2	-	DDVDH-0.2	

6.Timing Characteristics.

6.1 Reset Timing Characteristics.



Signal	Symbol	Parameter	Min	Max	Unit
RESX	tRW	Reset pulse duration	10		μs
	tRT	Reset cancel		5 (note 1,5)	ms
				120 (note 1,6,7)	ms

Note 1: The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NV memory to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.

Note 2: Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below: -

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 10us	Reset
Between 5us and 10us	Reset starts

Note 3: During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out -mode. The display remains the blank state in Sleep In -mode.) And then return to Default condition for Hardware Reset.

Note 4: Spike Rejection also applies during a valid reset pulse as shown below:



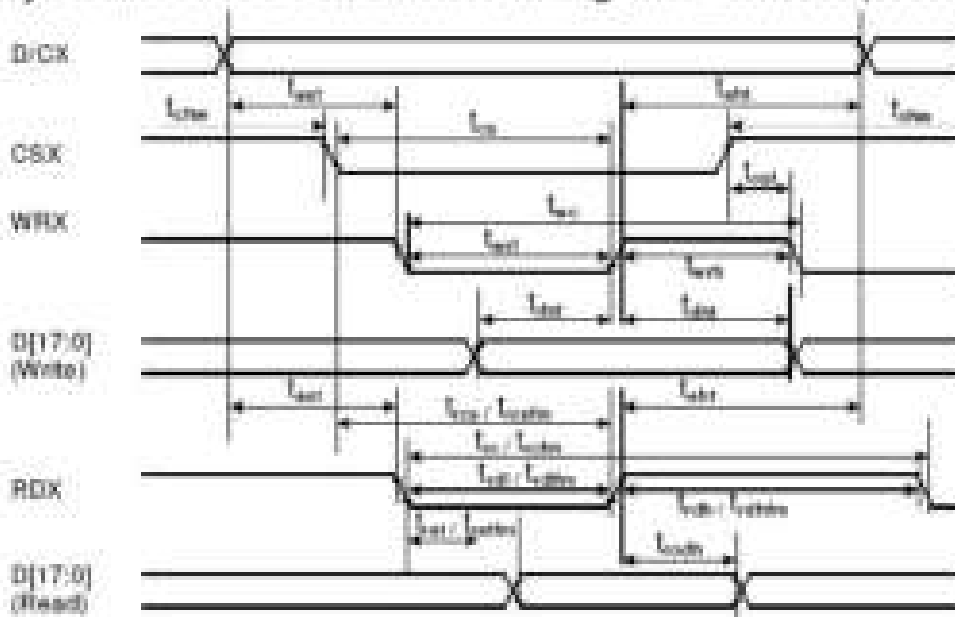
Note 5: When Reset applied during Sleep In Mode.

Note 6: When Reset applied during Sleep Out Mode.

Note 7: It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

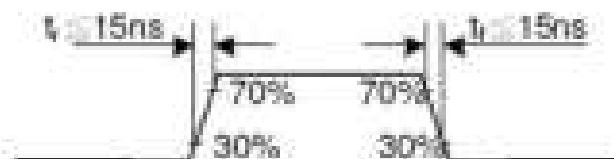
6.2. i80-System Interface Timing Characteristics.

Display Parallel 18/16/9/8-bit Interface Timing Characteristics (8080-1 system)

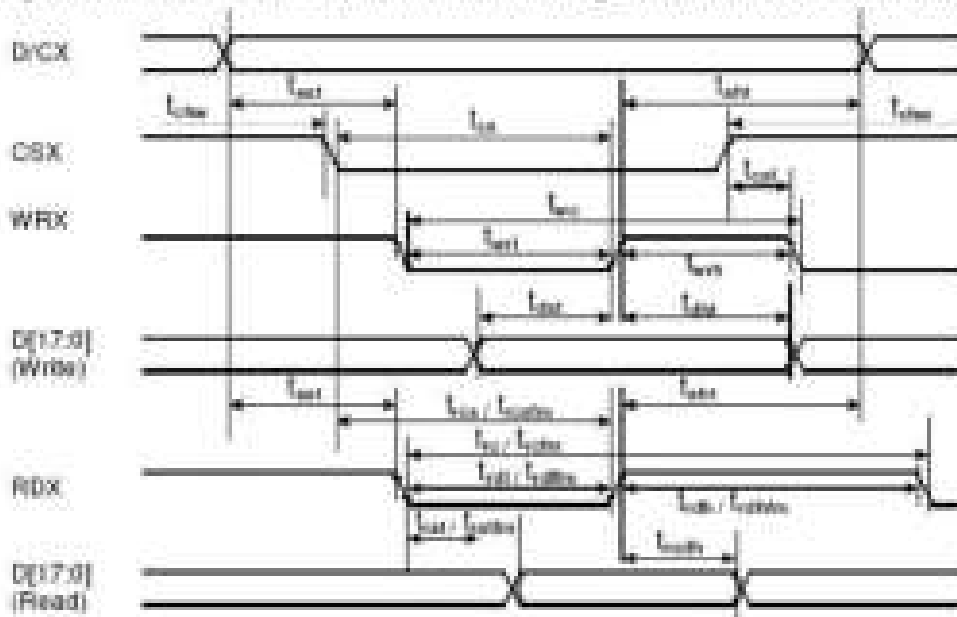


Signal	Symbol	Parameter	min	max	Unit	Description
D/CX	t _{setup}	Address setup time	0	-	ns	
	t _{hold}	Address hold time (Write/Read)	0	-	ns	
CSX	t _{ch}	CSX "H" pulse width	0	-	ns	
	t _{cs}	Chip Select setup time (Write)	15	-	ns	
	t _{rcs}	Chip Select setup time (Read ID)	45	-	ns	
	t _{rcsfm}	Chip Select setup time (Read FM)	355	-	ns	
	t _{wait}	Chip Select Wait time (Write/Read)	10	-	ns	
	t _{wd}	Write data setup time	10	-	ns	
WFX	t _{wc}	Write cycle	65	-	ns	
	t _{wrh}	Write Control pulse H duration	15	-	ns	
	t _{wrl}	Write Control pulse L duration	15	-	ns	
RDX (FM)	t _{rdm}	Read Cycle (FM)	450	-	ns	
	t _{rdhm}	Read Control H duration (FM)	90	-	ns	
	t _{rdlm}	Read Control L duration (FM)	355	-	ns	
RDX (ID)	t _{rd}	Read cycle (ID)	160	-	ns	
	t _{rdh}	Read Control pulse H duration	90	-	ns	
	t _{rdl}	Read Control pulse L duration	45	-	ns	
D[17:0], D[15:0], D[9:0], D[7:0]	t _{dwl}	Write data setup time	10	-	ns	For maximum CL=30pF For minimum CL=6pF
	t _{dwh}	Write data hold time	10	-	ns	
	t _{rat}	Read access time	-	40	ns	
	t _{rafm}	Read access time	-	340	ns	
	t _{rod}	Read output disable time	20	80	ns	

Note: T_a = -30 to 70 °C, V_{DDI} = 1.65V to 3.3V, V_{CI} = 2.5V to 3.3V, V_{SS} = 0V

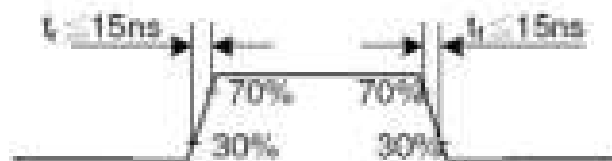


Display Parallel 18/16/9/8-bit Interface Timing Characteristics(8080- II system)



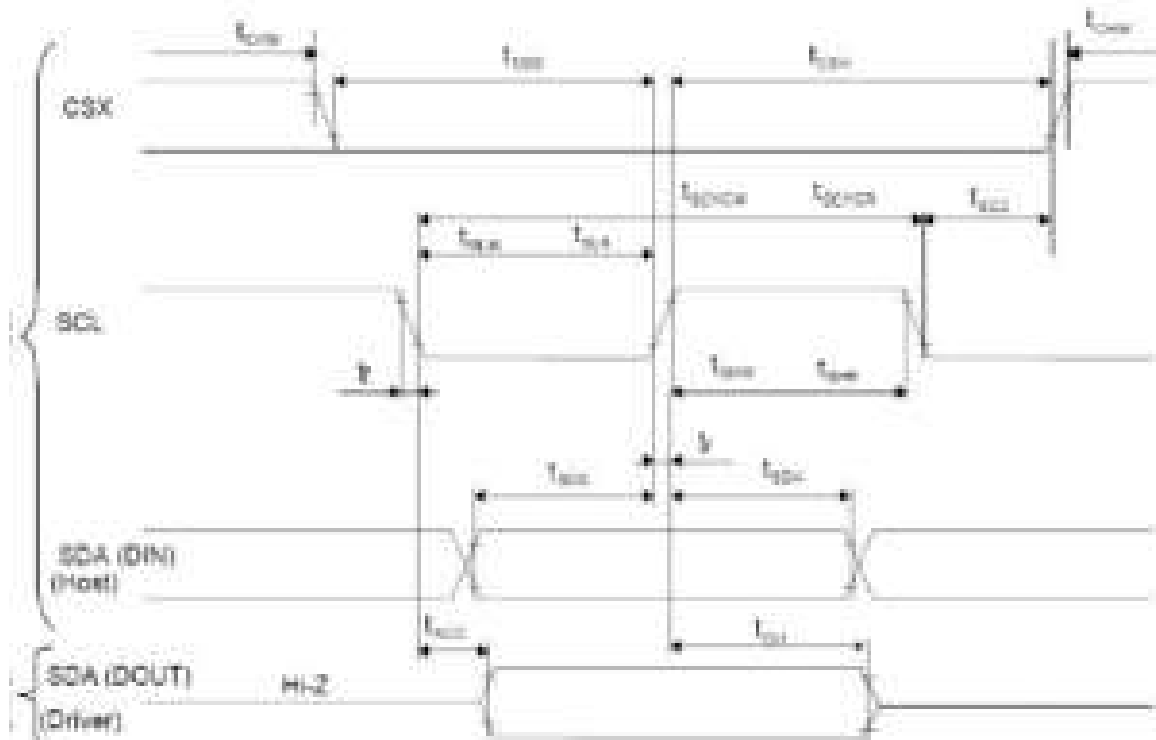
Signal	Symbol	Parameter	min	max	Unit	Description
DCX	t _{set}	Address setup time	0	-	ns	
	t _{shd}	Address hold time (Write/Read)	0	-	ns	
CSX	t _{chw}	CSX 'H' pulse width	0	-	ns	
	t _{cs}	Chip Select setup time (Write)	15	-	ns	
	t _{ccs}	Chip Select setup time (Read ID)	45	-	ns	
	t _{cdm}	Chip Select setup time (Read FM)	355	-	ns	
	t _{cd}	Chip Select Wait time (Write/Read)	10	-	ns	
	t _{cc}	Write cycle	66	-	ns	
WRX	t _{wrh}	Write Control pulse H duration	15	-	ns	
	t _{wrl}	Write Control pulse L duration	15	-	ns	
	t _{wc}	Write cycle	66	-	ns	
RDX (FM)	t _{rdm}	Read Cycle (FM)	450	-	ns	
	t _{rchh}	Read Control H duration (FM)	90	-	ns	
	t _{rdl}	Read Control L duration (FM)	355	-	ns	
RDX (ID)	t _{rc}	Read cycle (ID)	160	-	ns	
	t _{rch}	Read Control pulse H duration	90	-	ns	
	t _{rdl}	Read Control pulse L duration	45	-	ns	
D[17:0], D[17:10]AO(8:1), D[17:10], D[17:0]	t _{dst}	Write data setup time	10	-	ns	For maximum CL=30pF For minimum CL=8pF
	t _{dst}	Write data hold time	10	-	ns	
	t _{dat}	Read access time	-	40	ns	
	t _{rdm}	Read access time	-	340	ns	
	t _{rd}	Read output disable time	20	80	ns	

Note: T_a = -30 to 70 °C; VDD=1.65V to 3.3V, VCC=2.5V to 3.3V, VSS=0V.



6.3. SPI Interface Timing Characteristics.

Display Serial Interface Timing Characteristics (3-line SPI system)

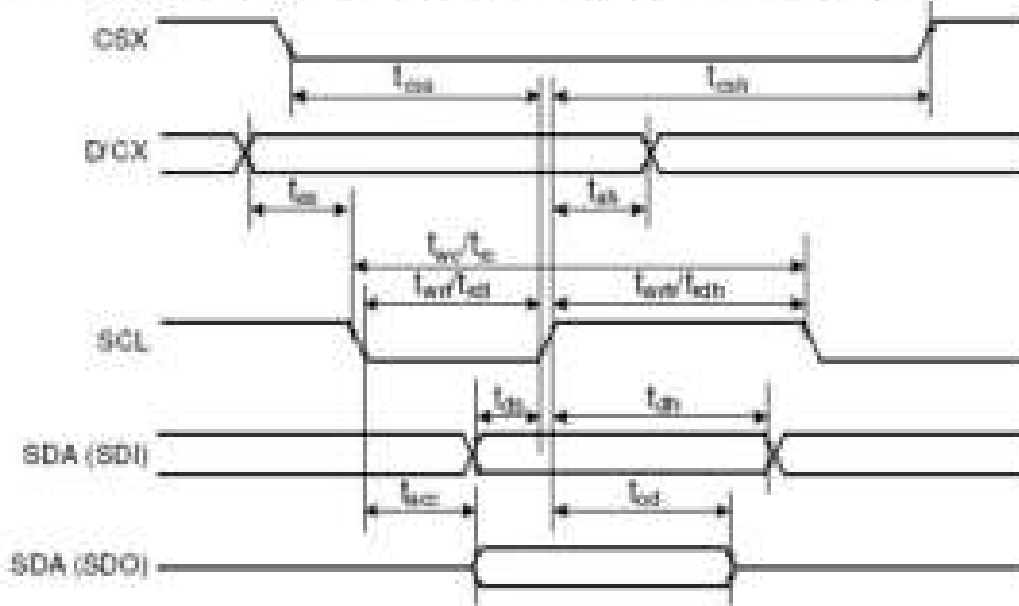


Signal	Symbol	Parameter	min	max	Unit	Description
SCL	tscw	Serial Clock Cycle (Write)	100	-	ns	
	tslw	SCL "H" Pulse Width (Write)	40	-	ns	
	tsllw	SCL "L" Pulse Width (Write)	40	-	ns	
	tscrr	Serial Clock Cycle (Read)	150	-	ns	
	tsrh	SCL "H" Pulse Width (Read)	60	-	ns	
	tsrl	SCL "L" Pulse Width (Read)	60	-	ns	
SDA / SCl (Input)	tads	Data setup time (Write)	30	-	ns	
	tadh	Data hold time (Write)	30	-	ns	
SDA / SDO (Output)	tacc	Access time (Read)	10	-	ns	
	tch	Output disable time (Read)	10	50	ns	
CSX	tscs	SCL-CSX	20	-	ns	
	tcsrh	CSX "H" Pulse Width	40	-	ns	
	tcss	CSX-SCL Time	60	-	ns	
	tcssh		65	-	ns	

Note: $T_A = 25^\circ\text{C}$, $V_{DD1}=1.65\text{V}$ to 3.3V , $V_{CL}=2.5\text{V}$ to 3.3V , $\text{AGND}=\text{VSS}=0\text{V}$

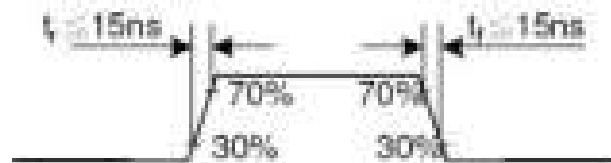


Display Serial Interface Timing Characteristics (4-line SPI system)

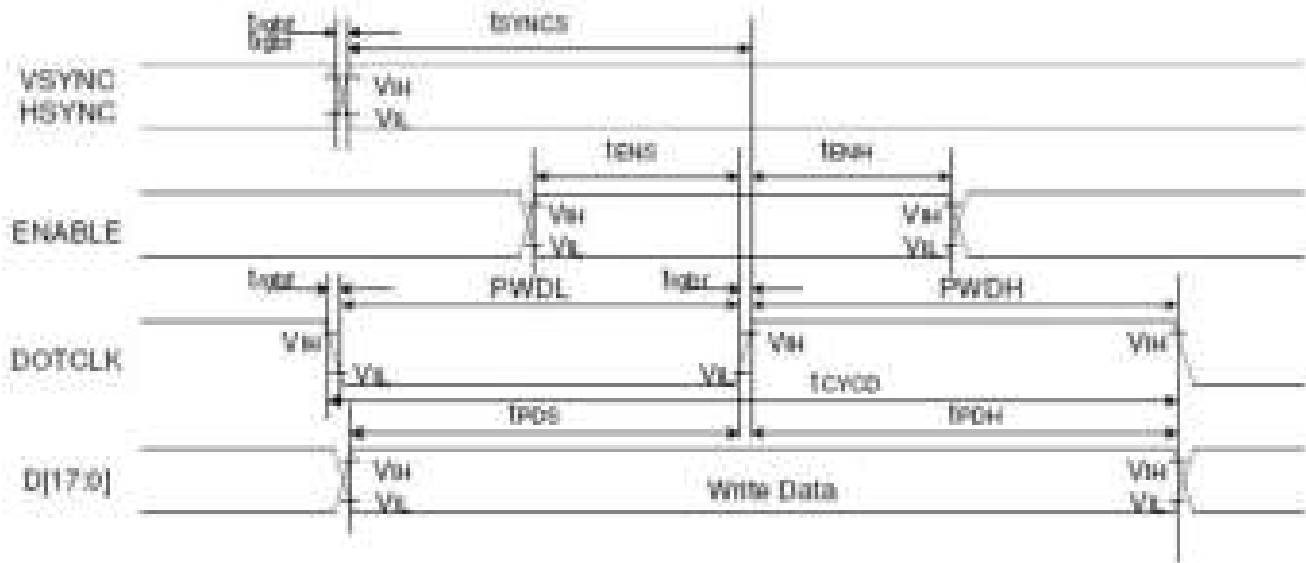


Signal	Symbol	Parameter	min	max	Unit	Description
CSX	t_{cs}	Chip select time (Write)	40	-	ns	
	t_{csh}	Chip select hold time (Read)	40	-	ns	
SCL	t_{wc}	Serial clock cycle (Write)	100	-	ns	
	t_{wh}	SCL 'H' pulse width (Write)	40	-	ns	
	t_{wl}	SCL 'L' pulse width (Write)	40	-	ns	
	t_{rc}	Serial clock cycle (Read)	150	-	ns	
	t_{rh}	SCL 'H' pulse width (Read)	60	-	ns	
	t_{rl}	SCL 'L' pulse width (Read)	60	-	ns	
D/CX	t_{dc}	D/CX setup time	10	-		
	t_{dch}	D/CX hold time (Write / Read)	10	-		
SDA / SDI (Input)	t_{ds}	Data setup time (Write)	30	-	ns	
	t_{dh}	Data hold time (Write)	30	-	ns	
SDA / SDO (Output)	t_{oc}	Access time (Read)	10	-	ns	For maximum $C_L=30pF$
	t_{od}	Output disable time (Read)	10	50	ns	For minimum $C_L=8pF$

Note: $T_a = 25^\circ C$, $V_{DDI}=1.85V$ to $3.3V$, $V_{CI}=2.5V$ to $3.3V$, $AGND=V_{SS}=0V$



6.4. RGB Interface Timing Characteristics.

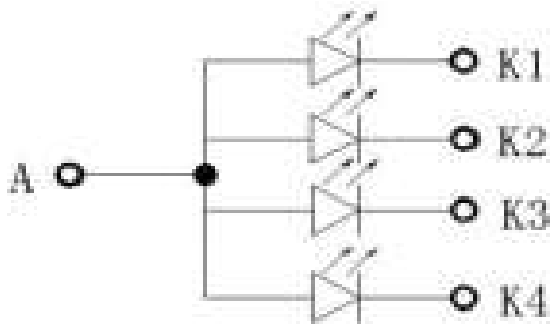


Signal	Symbol	Parameter	min	max	Unit	Description
VSYNC/ HSYNC	t_{suvs}	VSYNC/HSYNC setup time	15	-	ns	18/16-bit bus RGB interface mode
	t_{hvs}	VSYNC/HSYNC hold time	15	-	ns	
DE	t_{su}	DE setup time	15	-	ns	
	t_{hu}	DE hold time	15	-	ns	
D[17:0]	t_{su}	Data setup time	15	-	ns	
	t_{hu}	Data hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level period	15	-	ns	
	PWDL	DOTCLK low-level period	15	-	ns	
	t_{cyc}	DOTCLK cycle time	100	-	ns	
	t_{su}, t_{hf}	DOTCLK, HSYNC, VSYNC rise/fall time	-	15	ns	
VSYNC/ HSYNC	t_{suvs}	VSYNC/HSYNC setup time	15	-	ns	6-bit bus RGB interface mode
	t_{hvs}	VSYNC/HSYNC hold time	15	-	ns	
DE	t_{su}	DE setup time	15	-	ns	
	t_{hu}	DE hold time	15	-	ns	
D[17:0]	t_{su}	Data setup time	15	-	ns	
	t_{hu}	Data hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level pulse period	15	-	ns	
	PWDL	DOTCLK low-level pulse period	15	-	ns	
	t_{cyc}	DOTCLK cycle time	100	-	ns	
	t_{su}, t_{hf}	DOTCLK, HSYNC, VSYNC rise/fall time	-	15	ns	

Note: $T_a = -30$ to 70 °C, $V_{DD}=1.85V$ to $3.3V$, $V_{CI}=2.5V$ to $3.3V$, $AGND=VSS=0V$



7. Backlight Characteristics.



Item	Symbol	MIN	TYP	MAX	UNIT	Test Condition	Note
Supply Voltage	Vf	3.0	3.2	3.4	V	If=60 mA	-
Supply Current	If	-	60	-	mA	-	-
Reverse Voltage	Vr	-	-	5	V	10uA	
Power dissipation	Pd	-	192	-	mW	-	
Luminous Intensity for LCM		-	320	-	Cd/m²	If=60 mA	
Uniformity for LCM	-	80	-	-	%	If=60 mA	
Life Time	-	50000	-	-	Hr	If=60 mA	-
Backlight Color	White						

8.Optical Characteristics

Item		Symbol	Conditions	Specifications	Unit	Note
Transmittance		T%	Viewing normal angle $\theta_v = 0^\circ$	6.0	%	All left side data are based on GMD's following condition - 1.LCD : NTSC 60% 2.LC : TN 3.Light Source : CM LED BLU 4.Film : Nitro Linear Polarizer 5.Machine : DMD
Contrast Ratio		CR		305	—	
Response Time (by Quick)		T _{on} , T _{off}		30	ms	
Viewing Angle	Hor.	θ_{90}	Center C/R=10	45	deg	
		θ_{50}		45		
	Ver.	θ_{90}		45		
		θ_{50}		20		
CF only Chromaticity	Red	X_R	Viewing normal angle $\theta_v = 0^\circ$	0.635	—	Under C light Simulation
		Y_R		0.317	—	
	Green	X_G		0.209	—	
		Y_G		0.564	—	
	Blue	X_B		0.130	—	
		Y_B		0.116	—	
	White	X_w		0.298	—	
		Y_w		0.328	—	

*Note (1) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

$$\text{Contrast Ratio (CR)} = L_{63} / L_0$$

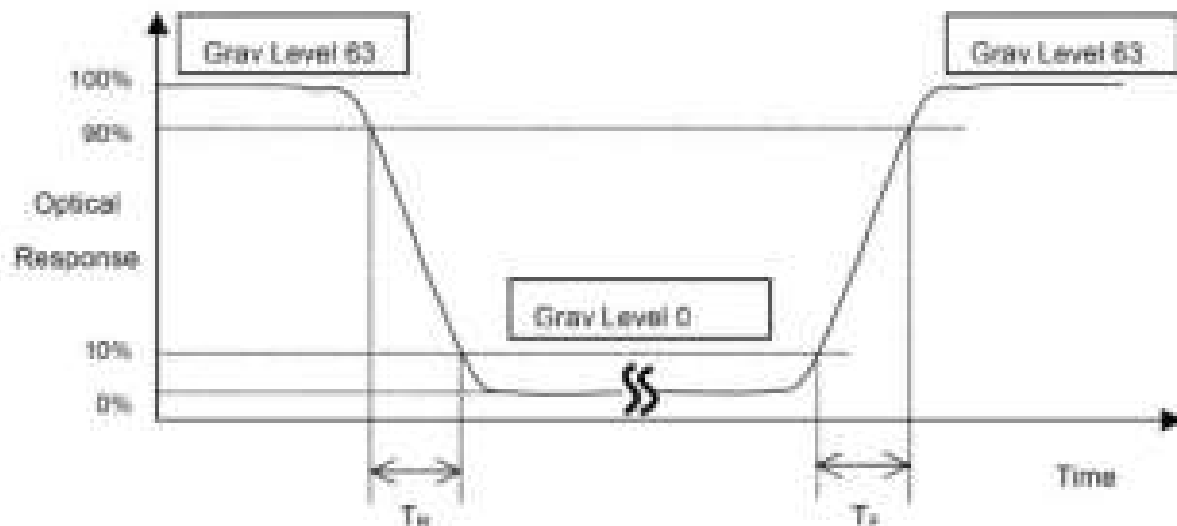
L₆₃: Luminance of gray level 63

L₀: Luminance of gray level 0

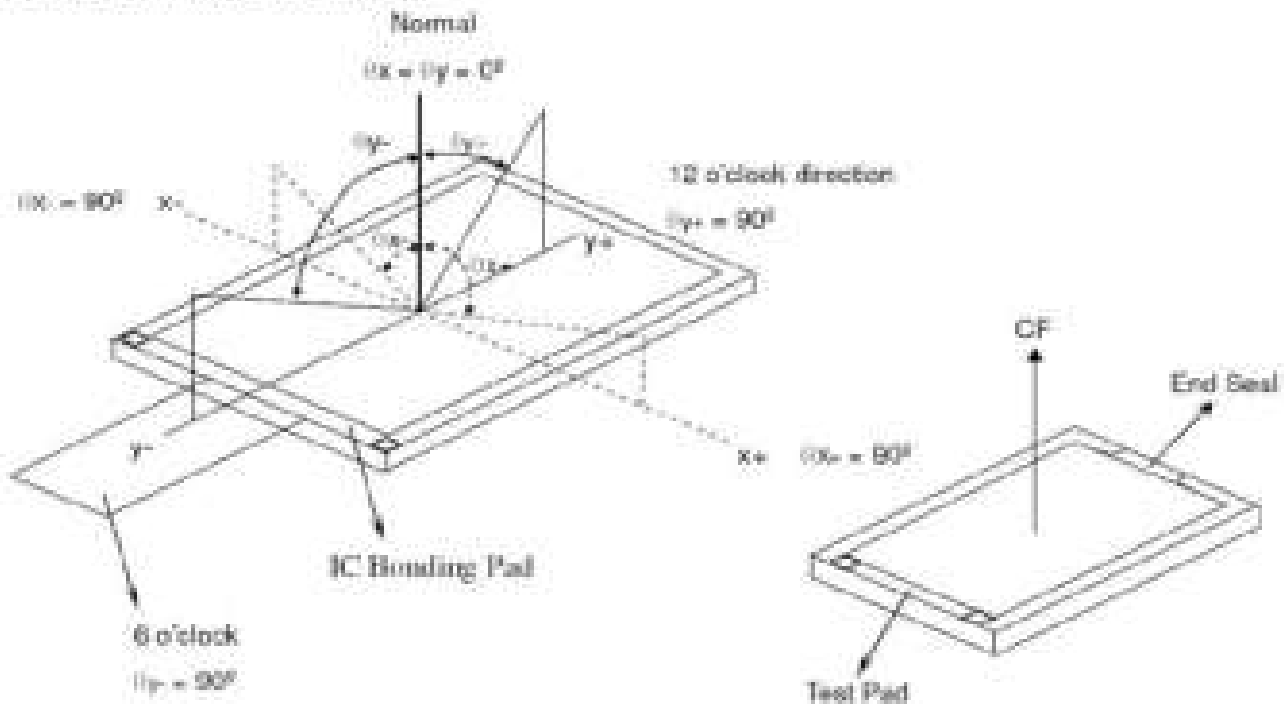
$$CR = CR (5)$$

CR (X) is corresponding to the Contrast Ratio of the point X at Figure in Note (5).

*Note (2) Definition of Response Time (TR, TF):



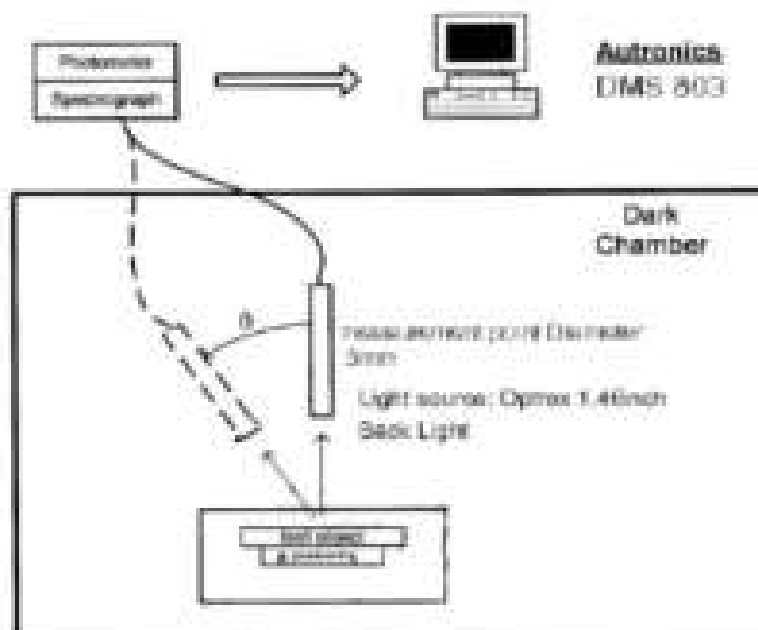
*Note(3) Definition of Viewing Angle



*** The above "Viewing Angle" is the measuring position with Largest Contrast Ratio, not for good image quality. View Direction for good image quality is 6 O'clock. Module maker can increase the "Viewing Angle" by applying Wide View Film.

*Note (4) Measurement Set-Up:

The LCD module should be stabilized at a given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 20 minutes in a windless room.



9. RELIABILITY

No.	Test Item	Test Condition	Remark
1	High Temperature Storage	+80℃± 2℃, 96 hrs	Note
2	Low Temperature Storage	-30℃± 2℃, 96 hrs	Note
3	High Temperature Operation	+70℃± 2℃, 96 hrs	Note
4	Low Temperature Operation	+20℃± 2℃, 96 hrs	Note
5	High Temperature & High Humidity Storage Test	+50℃± 5℃, 90%R.H, 96 hours	Note
6	Temperature Cycle (non operation)	-30℃ ← +25℃ → +80℃ (30mins ← 5mins → 30mins) 10 Cycles	Note
7	Electronic Static Discharge	Air Discharge: 2KV to with 5 times	Discharge for each polarity Mode of Operation: Single Discharge, successive discharge at least 1 sec
		Ambiance: 15℃~35℃, 30%~60%R.H Resistance(Rd): 330Ω ±10% Capacitance(Cs + Cd): 150pF±10%	
8	Vibration (Packaged)	Frequency range: 10Hz ~ 55 Hz Amplitude: 1.5mm Direction of X.Y. Z for 3 Hrs in total	
9	Drop Test (Packaged)	Height: 80cm, Time: 1 1 corner, 3 edged, 6 surfaces	

Note : Recovery Time should be 2~4 hours at room temperature (20±8℃) and humidity (below 60% R.H). No abnormalities in functions and appearance

10.INSPECTION CRITERION

10.1 Scope

Display Quality Evaluation

Mechanics Specification

10.2 Sampling Plan

MIL-STD-105E

Unless there is other agreement, the sampling plan for incoming inspection shall follow MIL-STD-105E

Lot size: Quantity per shipment as one lot (different model as different lot).

Sampling type: Normal inspection, single sampling

Sampling level: Level II.

10.3 Acceptable Quality Level

Item	Major	Minor
Appearance	1.0%	1.5%
Electrical	0.65	1.0%

10.3.1 Classification of defects:

10.3.1.1 Major defect

Any defect may result in functional failure, or reduce the usability of product for its purpose. For

Example: Electrical failure, deformation and etc.

10.3.1.2 Minor defect

The criteria on major or minor judgment will be according with the classification of defects.

10.4 Panel Inspection Condition

10.4.1 Environment:

10.4.2 Room Temperature: $25 \pm 5^{\circ} \text{C}$.

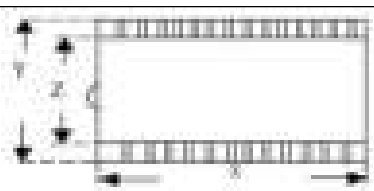
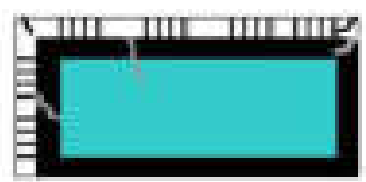
10.4.3 Humidity: $50 \pm 20\% \text{ RH}$.

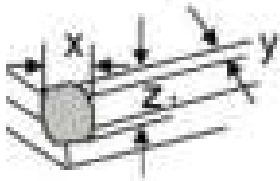
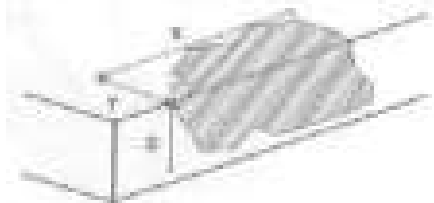
Illumination: 300 ~ 700 Lux.

10.4.4 Inspection Distance: $35 \pm 5 \text{ cm}$

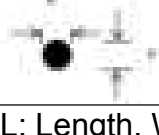
10.5 TFT Inspection Criteria

10.5.1 Visual inspection criterion in cosmetic / appearance

Glass defect			
N o	Item	Criteria	Remark
1	Dimension (Minor)	By engineering diagram	
2	Crack (Major)	Extensive crack	

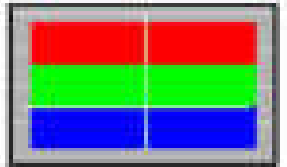
3	Corner (Minor)	$X \leq 3 \text{ mm}$ $Y \leq 3 \text{ mm}$ $Z \leq T$ Ignore	 T: Glass thickness Z: Thickness X: Length Y: Width
4	Side (Minor)	$X \leq 5 \text{ mm}$ $Y \leq 3 \text{ mm}$ $Z \leq T$ Ignore	 T: Glass thickness Z: Thickness X: Length Y: Width

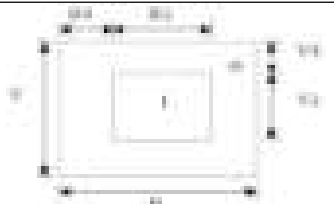
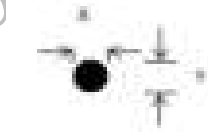
TFT defect in appearance

No	Item	Criteria	Remark
1	Foreign Spot (Minor) Including: Black spot, White spot Pin hole Foreign particle	$D \leq 0.15 \text{ mm}$, Ignore $0.15 \text{ mm} < D \leq 0.3 \text{ mm}$, $N \leq 3$ $0.3 \text{ mm} < D$, $N = 0$ Distance $\geq 5 \text{ mm}$ Ignore if out of Area AA	$D = (X+Y)/2$, X: Length, Y: Width 
2	Foreign Line(Minor) Including: Black line White line Bright line	$W \leq 0.03 \text{ mm}$, Ignore $0.03 \text{ mm} < W \leq 0.05 \text{ mm}$, $L \leq 4 \text{ mm}$, $N \leq 3$ $0.05 \text{ mm} < W \leq 0.08 \text{ mm}$, $L \leq 4 \text{ mm}$, $N \leq 1$ $W > 0.08 \text{ mm}$, $N = 0$ Ignore if out of Area AA	L: Length, W: Width 
3	Polarizer Dent/Air Bubble (Minor)	$D \leq 0.2 \text{ mm}$, Ignore $0.2 \text{ mm} < D \leq 0.3 \text{ mm}$, $N \leq 3$ $0.3 \text{ mm} < D \leq 0.5 \text{ mm}$, $N \leq 1$ $D > 0.50 \text{ mm}$, $N = 0$ Distance $\geq 5 \text{ mm}$	$D = (X+Y)/2$, X: Length, Y: Width 
4	Polarizer Scratches (Minor)	$W \leq 0.03 \text{ mm}$, Ignore $0.03 \text{ mm} < W \leq 0.05 \text{ mm}$, $L \leq 4 \text{ mm}$, $N \leq 3$ $0.05 \text{ mm} < W \leq 0.08 \text{ mm}$, $L \leq 4 \text{ mm}$, $N \leq 1$ $W > 0.08 \text{ mm}$, $N = 0$ Ignore if out of Area AA	L: Length, W: Width 

Other defects			
No	Item	Criteria	Remark
1	FPC (Minor)	Any crack or breakage which effect the function are not allowed Disregard if the dirty removed	
2	Backlight (Minor)	Power up is allowed. Breaking off is not allowed. The scratch which may causes a problem in practical use is not allowed	
3	Bezel (Minor)	Erasable dirt is ignore	

10.5.2 Visual inspection criterion in electrical display

Glass defect			
No	Item	Criteria	Remark
1	No display (Major) Abnormally Short circuit	Not allowed	
2	Missing line (Major)	Not allowed	
3	Darker or lighter line (Major)	Not allowed	
4	Weak line (Minor)	By limit sample	

Display Inspection						
No	Item	Criteria				Remark
1	Bright / Dark dot	Items	Area I	Area O	Tota I	 1.1sub-pixel: 1R or 1G or 1B 2.Point defect area ≥ 1/2 sub pixel
		Bright	1	1	1	
		Dark	1	3	3	
		Bright & Dark	2	3	4	
		2 adjacent dots	0	0	0	
		Minimum Distance ≥ 5mm				
2	Tiny bright dot	Visible through 6% ND filter D≤0.15mm, Ignore 0.15mm<D≤0.3mm, N≤3 0.3mm<D≤0.35mm, N≤1 D>0.35mm, N=0 Distance≥5mm Ignore if out of Area AA				D =(X+Y)/2, X: Length, Y: Width 
4	Mura/Waving/ Hot spot	Not visible through 6% ND filter in 50% gray or judge by limit sample if necessary				

* Note:

- Defect which is on the Black Matrix (outside of active area) are not considered as a defect.
- If any specific defect is not included in the above defect table, this defect should be judged by Formike.
- W: Width, L: Length D: Average Diameter N: Count.

11. PRECAUTION RELATING & PRODUCT HANDLING

Display is assembled and adjusted with a high degree of precision. Do not attempt to make any alteration or modification.

11.1 SAFETY

11.1.1 If the LCD panel breaks, be careful not to get the liquid crystal to touch your skin.

11.1.2 If the liquid crystal touches your skin or clothes, please wash it off immediately by using soap and water.

11.2 HANDLING

11.2.1 Avoid any strong mechanical shock which can break the glass.

11.2.2 Avoid static electricity which can damage the CMOS LSI - When working with the module, be sure to ground your body and any electrical equipment you may be using. The followings should be noted:

11.2.2.1 CMOS-LSI is used for the module circuit; therefore operators should be grounded whenever he/she comes into contact with the module.

11.2.2.2 Do not touch any of the conductive parts such as the LSI pads; the copper leads on the PCB and the interface terminals with any parts of the human body.

11.2.2.3 Do not touch the connection terminals of the display with bare hand; it will cause disconnection or defective insulation of terminals.

11.2.2.4 The modules should be kept in anti-static bags or other containers resistant to static for storage.

11.2.2.5 Only properly grounded soldering irons should be used.

11.2.2.6 If an electric screwdriver is used, it should be grounded and shielded to prevent sparks.

11.2.2.7 The normal static prevention measures should be observed for work clothes and working benches.

11.2.3.8 Since dry air is inductive to static, a relative humidity of 50-60% is recommended

11.2.3 Do not remove the panel or frame from the module.

11.2.4 The polarizing plate of the display is very fragile. Please handle it very carefully, do not touch, push or rub the exposed polarizing with anything harder than an HB pencil lead (glass, tweezers, etc.)

11.2.5 Do not wipe the polarizing plate with a dry cloth, as it may easily scratch the surface of plate.

11.2.6 Do not touch the display area with bare hands, this will stain the display area.

11.2.7 Do not use ketonics solvent & aromatic solvent. Use with a soft cloth soaked with a cleaning naphtha solvent.

11.2.8 To control temperature and time of soldering is $300 \pm 10^{\circ}\text{C}$ and 3-4 sec.

To avoid liquid (include organic solvent) stained on LCD Module.

11.3 STORAGE

11.3.1 Store the panel or module in a dark place where the temperature is $25^{\circ}\text{C} \pm 5^{\circ}\text{C}$ and the humidity is below 60% RH.

11.3.2 Avoid exposure to direct sunlight or to the light of fluorescent lamps.

11.3.3 Do not place the module near organic solvents or corrosive gases.

Do not crush, shake, or jolt the module.

11.4 LIMITED WARRANTY

11.4.1 FORMIKE modules are not consumer products, but may be incorporated by FORMIKE's customers into consumer products or components thereof, FORMIKE does not warrant that its modules and components are fit for any such particular purpose.

11.4.2 The liability of FORMIKE is limited to repair or replacement on the terms set forth below. FORMIKE will not be responsible for any subsequent or consequential events or injury or damage to any personnel or user including third party personnel and/or user. Unless otherwise agreed in writing between FORMIKE and the customer, FORMIKE will only replace or repair any of its Modules which is found defective electrically or visually when inspected in accordance with FORMIKE INSPECTION CRITERIA

11.4.3 No warranty can be granted if any of the precautions state in handling liquid crystal display has been disregarded. Broken glass, scratches on polarizer mechanical damages as well as defects that are caused accelerated environment tests are excluded from warranty.

11.4.4 In returning the modules, they must be properly packaged; there should be detailed description of the failures or defect.

12. OTHERS

12.1 If there is any not specified quality standard in this specification as well as RMA , please refer to < INSPECTION CRITERIA>. Contact FORMIKE to get the complete <INSPECTION CRITERIA> by the contact window or feedback@wandisplay.com.

12.2 Special agreement of <INSPECTION CRITERIA> is recognized only in writhing between FORMIKE and the customer also indicated it before ordering.