



8-/16-Channel, 3 V/5 V, Serial Input, Single-Supply, 12-/14-Bit Voltage Output

Data Sheet

AD5390/AD5391/AD5392

FEATURES

AD5390: 16-channel, 14-bit voltage output DAC

AD5391: 16-channel, 12-bit voltage output DAC

AD5392: 8-channel, 14-bit voltage output DAC

Guaranteed monotonic

INL

±1 LSB max (AD5391)

±3 LSB max (AD5390-5/AD5392-5)

±4 LSB max (AD5390-3/AD5392-3)

On-chip 1.25 V/2.5 V, 10 ppm/°C reference

Temperature range: -40°C to +85°C

Rail-to-rail output amplifier

Power-down mode

Package types

64-lead LFCSP (9 mm × 9 mm)

52-lead LQFP (10 mm × 10 mm)

User interfaces

Serial SPI-, QSPI-, MICROWIRE-, and DSP-compatible

(featuring data readback)

I²C-compatible interface

Integrated functions

channel monitor

simultaneous output update via LDAC

clear function to user-programmable code

amplifier boost mode to optimize slew rate

user-programmable offset and gain adjust

toggle mode enables square wave generation

thermal monitor

Robust 6.5 kV HBM and 2 kV FICDM ESD rating

APPLICATIONS

Instrumentation and industrial control

Power amplifier control

Level setting (ATE)

Control systems

Microelectromechanical systems (MEMs)

Variable optical attenuators (VOAs)

Optical transceivers (MSA 300, XFP)

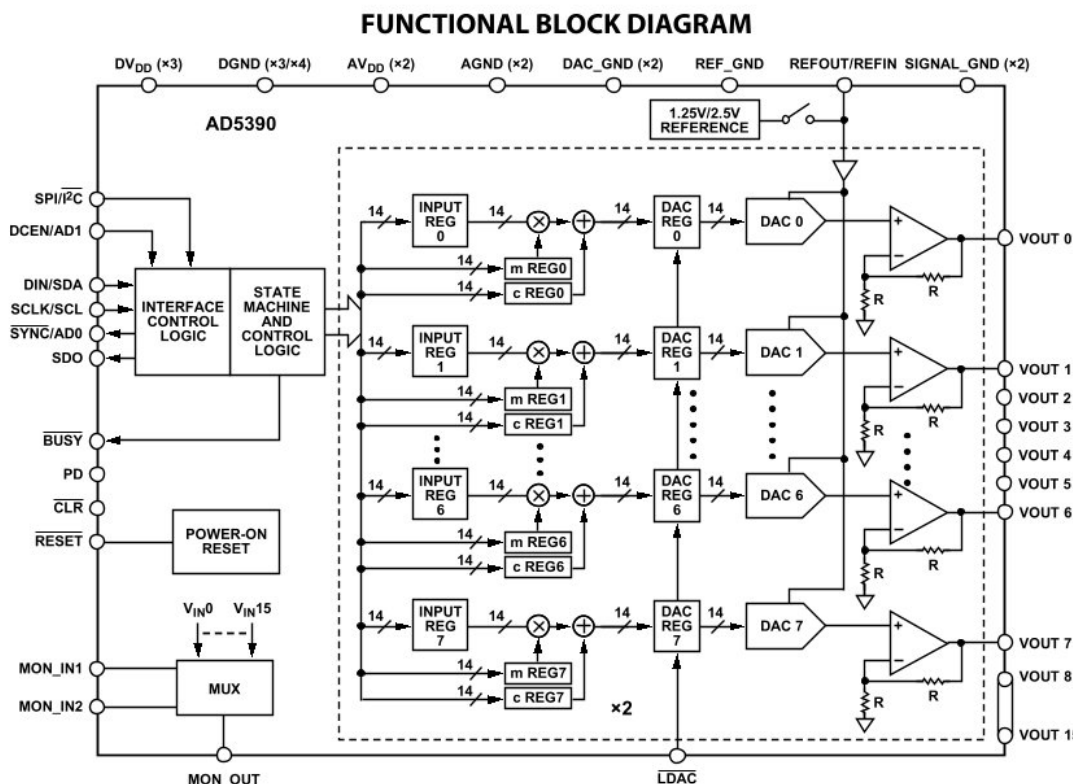


Figure 1.

Rev. F

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TABLE OF CONTENTS

Features	1	I ² C Write Operation	28
Applications.....	1	4-Byte Mode.....	28
Functional Block Diagram	1	3-Byte Mode.....	29
Revision History	3	2-Byte Mode.....	30
General Description.....	4	AD5390/AD5391/AD5392 On-Chip Special Function	
Specifications.....	5	Registers.....	31
AD5390-5/AD5391-5/AD5392-5 Specifications	5	Control Register Write.....	33
AD5390-5/AD5391-5/AD5392-5 AC Characteristics.....	7	Hardware Functions.....	35
AD5390-3/AD5391-3/AD5392-3 Specifications	8	Reset Function	35
AD5390-3/AD5391-3/AD5392-3 AC Characteristics.....	10	Asynchronous Clear Function.....	35
Timing Characteristics.....	11	$\overline{\text{BUSY}}$ and $\overline{\text{LDAC}}$ Functions.....	35
Serial SPI-, QSPI-, MICROWIRE-, and DSP-Compatible		Power-On Reset	35
Interface	11	Power-Down	35
I ² C Serial Interface.....	13	Microprocessor Interfacing.....	35
Absolute Maximum Ratings.....	14	Application Information.....	37
ESD Caution.....	14	Power Supply Decoupling	37
Pin Configuratons and Function Descriptions	15	Power Supply Sequencing	38
Terminology	18	Typical Configuration Circuit	39
Typical Performance Characteristics	19	AD5390/AD5391/AD5392 Monitor Function.....	40
Functional Description	23	Toggle Mode Function.....	40
DAC Architecture.....	23	Thermal Monitor Function.....	40
Data Decoding	24	Outline Dimensions	42
Interfaces.....	25	Ordering Guide	43
DSP-, SPI-, and MICROWIRE-Compatible Serial Interface.....	25		
I ² C Serial Interface.....	27		

REVISION HISTORY**6/14—Rev. E to Rev. F**

Deleted Table 1; Renumbered Sequentially	4
Changed AD5390-3/AD5391-3/AD5392-3 Input Current from $\pm 10 \mu\text{A}$ (max) to $\pm 1 \mu\text{A}$ (max); Table 3	8
Changes to Table 5	11
Changes to Soft Reset Section	31
Changes to Reset Function Section	35
Replaced ADSP2101 with ADSP-BF527	36
Added Power Supply Sequencing Section	38
Changes to Ordering Guide	43

6/12—Rev. D to Rev. E

Changes to Table 1	4
Change to Accuracy Parameter, Gain Error, Table 2	5
Change to Accuracy Parameter, Gain Error, Table 4	8
Added Exposed Pad Notation to Figure 7 and Figure 8	15

5/12—Rev. C to Rev. D

Changes to Product Title and Features Section	1
Changes to Table 2	4
Changes to Table 3	6
Changes to Table 4	7
Changes to Table 5	9
Changes to Table 6	10
Changes to Table 8	13
Changes to Figure 8 and Figure 10	14
Changes to Table 9	16
Changes to Figure 17, Figure 18, Figure 19, And Figure 22	19
Changes to Figure 23, Figure 24, Figure 25, and Figure 26	20
Changes to Table 26	32
Changes to Ordering Guide	40

1/09—Rev. B to Rev. C

Updated Format	Universal
Changes to Figure 33	27
Added Figure 34 and Renumbered Sequentially	27
Changes to Figure 34	28
Changes to Table 28	33
Change order of Figure 41 and Figure 42	36
Changes to Toggle Mode Function Section	37

3/06—Rev. A to Rev. B

Changes to Figure 1	1
Changes to Table 9	14
Changes to Table 12 and Table 15	23
Updated Outline Dimensions	39
Changes to Ordering Guide	40

10/04—Rev. 0 to Rev. A

Changes to Features	1
Changes to Table 1	3
Changes to Table 2	4
Changes to Table 3	6
Changes to Table 4	7
Changes to Figure 36	35
Changes to Figure 37	36
Changes to Figure 38	36
Changes to Ordering Guide	41

4/04—Revision 0: Initial Version

GENERAL DESCRIPTION

The [AD5390/AD5391](#) are complete single-supply, 16-channel, 14-bit and 12-bit DACs, respectively. The [AD5392](#) is a complete single-supply, 8-channel, 14-bit DAC. The devices are available in either a 64-lead LFCSP or a 52-lead LQFP. All channels have an on-chip output amplifier with rail-to-rail operation. All devices include an internal 1.25/2.5 V, 10 ppm/°C reference, an on-chip channel monitor function that multiplexes the analog outputs to a common MON_OUT pin for external monitoring, and an output amplifier boost mode that optimizes the output amplifier slew rate.

The [AD5390/AD5391/AD5392](#) contain a 3-wire serial interface with interface speeds in excess of 30 MHz that are compatible with SPI®, QSPI™, MICROWIRE™, and DSP interface standards and an I²C-compatible interface supporting a 400 kHz data transfer rate.

An input register followed by a DAC register provides double-buffering, allowing DAC outputs to be updated independently or simultaneously using the LDAC input. Each channel has a programmable gain and offset adjust register, letting the user fully calibrate any DAC channel.

Power consumption is typically 0.25 mA per channel.