

**Module 1:
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Introduction

The Spartan®-3 family of Field-Programmable Gate Arrays is specifically designed to meet the needs of high volume, cost-sensitive consumer electronic applications. The eight-member family offers densities ranging from 50,000 to 5,000,000 system gates, as shown in [Table 1](#).

The Spartan-3 family builds on the success of the earlier Spartan-IIE family by increasing the amount of logic resources, the capacity of internal RAM, the total number of I/Os, and the overall level of performance as well as by improving clock management functions. Numerous enhancements derive from the Virtex®-II platform technology. These Spartan-3 FPGA enhancements, combined with advanced process technology, deliver more functionality and bandwidth per dollar than was previously possible, setting new standards in the programmable logic industry.

Because of their exceptionally low cost, Spartan-3 FPGAs are ideally suited to a wide range of consumer electronics applications, including broadband access, home networking, display/projection and digital television equipment.

The Spartan-3 family is a superior alternative to mask programmed ASICs. FPGAs avoid the high initial cost, the lengthy development cycles, and the inherent inflexibility of conventional ASICs. Also, FPGA programmability permits design upgrades in the field with no hardware replacement necessary, an impossibility with ASICs.

Table 1: Summary of Spartan-3 FPGA Attributes

Device	System Gates	Equivalent Logic Cells ⁽¹⁾	CLB Array (One CLB = Four Slices)			Distributed RAM Bits (K=1024)	Block RAM Bits (K=1024)	Dedicated Multipliers	DCMs	Max. User I/O	Maximum Differential I/O Pairs
			Rows	Columns	Total CLBs						
XC3S50 ⁽²⁾	50K	1,728	16	12	192	12K	72K	4	2	124	56
XC3S200 ⁽²⁾	200K	4,320	24	20	480	30K	216K	12	4	173	76
XC3S400 ⁽²⁾	400K	8,064	32	28	896	56K	288K	16	4	264	116
XC3S1000 ⁽²⁾	1M	17,280	48	40	1,920	120K	432K	24	4	391	175
XC3S1500	1.5M	29,952	64	52	3,328	208K	576K	32	4	487	221
XC3S2000	2M	46,080	80	64	5,120	320K	720K	40	4	565	270
XC3S4000	4M	62,208	96	72	6,912	432K	1,728K	96	4	633	300
XC3S5000	5M	74,880	104	80	8,320	520K	1,872K	104	4	633	300

Notes:

- Logic Cell = 4-input Look-Up Table (LUT) plus a 'D' flip-flop. "Equivalent Logic Cells" equals "Total CLBs" x 8 Logic Cells/CLB x 1.125 effectiveness.
- These devices are available in Xilinx Automotive versions as described in [DS314: Spartan-3 Automotive XA FPGA Family](#).

Features

- Low-cost, high-performance logic solution for high-volume, consumer-oriented applications
 - Densities up to 74,880 logic cells
- SelectIO™ interface signaling
 - Up to 633 I/O pins
 - 622+ Mb/s data transfer rate per I/O
 - 18 single-ended signal standards
 - 8 differential I/O standards including LVDS, RSDS
 - Termination by Digitally Controlled Impedance
 - Signal swing ranging from 1.14V to 3.465V
 - Double Data Rate (DDR) support
 - [DDR, DDR2 SDRAM support](#) up to 333 Mb/s
- Logic resources
 - Abundant logic cells with shift register capability
 - Wide, fast multiplexers
 - Fast look-ahead carry logic
 - Dedicated 18 x 18 multipliers
 - JTAG logic compatible with IEEE 1149.1/1532
- SelectRAM™ hierarchical memory
 - Up to 1,872 Kbits of total block RAM
 - Up to 520 Kbits of total distributed RAM
- Digital Clock Manager (up to four DCMs)
 - Clock skew elimination
 - Frequency synthesis
 - High resolution phase shifting
- Eight global clock lines and abundant routing
- Fully supported by [Xilinx ISE®](#) and [WebPACK™](#) software development systems
- [MicroBlaze™](#) and [PicoBlaze™](#) processor, [PCI®](#), [PCI Express® PIPE Endpoint](#), and other [IP cores](#)
- Pb-free packaging options
- Automotive [Spartan-3 XA Family](#) variant