

**Module 1:
Introduction and Ordering Information****DS529 (v2.1) December 18, 2018**

- Introduction
- Features
- Architectural and Configuration Overview
- General I/O Capabilities
- Production Status
- Supported Packages and Package Marking
- Ordering Information

**Module 2:
Spartan-3A FPGA Family: Functional
Description****DS529 (v2.1) December 18, 2018**

The functionality of the Spartan®-3A FPGA family is described in the following documents.

- [UG331: Spartan-3 Generation FPGA User Guide](#)
 - Clocking Resources
 - Digital Clock Managers (DCMs)
 - Block RAM
 - Configurable Logic Blocks (CLBs)
 - Distributed RAM
 - SRL16 Shift Registers
 - Carry and Arithmetic Logic
 - I/O Resources
 - Embedded Multiplier Blocks
 - Programmable Interconnect
 - ISE® Design Tools and IP Cores
 - Embedded Processing and Control Solutions
 - Pin Types and Package Overview
 - Package Drawings
 - Powering FPGAs
 - Power Management
- [UG332: Spartan-3 Generation Configuration User Guide](#)
 - Configuration Overview
 - Configuration Pins and Behavior
 - Bitstream Sizes
 - Detailed Descriptions by Mode
 - Master Serial Mode using Platform Flash PROM
 - Master SPI Mode using Commodity Serial Flash
 - Master BPI Mode using Commodity Parallel Flash
 - Slave Parallel (SelectMAP) using a Processor
 - Slave Serial using a Processor
 - JTAG Mode
 - ISE iMPACT Programming Examples
 - MultiBoot Reconfiguration
 - Design Authentication using Device DNA
- [UG334: Spartan-3A/3AN FPGA Starter Kit User Guide](#)

**Module 3:
DC and Switching Characteristics****DS529 (v2.1) December 18, 2018**

- DC Electrical Characteristics
 - Absolute Maximum Ratings
 - Supply Voltage Specifications
 - Recommended Operating Conditions
- Switching Characteristics
 - I/O Timing
 - Configurable Logic Block (CLB) Timing
 - Multiplier Timing
 - Block RAM Timing
 - Digital Clock Manager (DCM) Timing
 - Suspend Mode Timing
 - Device DNA Timing
 - Configuration and JTAG Timing

**Module 4:
Pinout Descriptions****DS529 (v2.1) December 18, 2018**

- Pin Descriptions
- Package Overview
- Pinout Tables
- Footprint Diagrams

For more information on the Spartan-3A FPGA family, go to www.xilinx.com/spartan3a

Spartan-3A FPGA	Status
XC3S50A	Production
XC3S200A	Production
XC3S400A	Production
XC3S700A	Production
XC3S1400A	Production

Introduction

The Spartan®-3A family of Field-Programmable Gate Arrays (FPGAs) solves the design challenges in most high-volume, cost-sensitive, I/O-intensive electronic applications. The five-member family offers densities ranging from 50,000 to 1.4 million system gates, as shown in [Table 1](#).

The Spartan-3A FPGAs are part of the Extended Spartan-3A family, which also include the non-volatile Spartan-3AN and the higher density Spartan-3A DSP FPGAs. The Spartan-3A family builds on the success of the earlier Spartan-3E and Spartan-3 FPGA families. New features improve system performance and reduce the cost of configuration. These Spartan-3A family enhancements, combined with proven 90 nm process technology, deliver more functionality and bandwidth per dollar than ever before, setting the new standard in the programmable logic industry.

Because of their exceptionally low cost, Spartan-3A FPGAs are ideally suited to a wide range of consumer electronics applications, including broadband access, home networking, display/projection, and digital television equipment.

The Spartan-3A family is a superior alternative to mask programmed ASICs. FPGAs avoid the high initial cost, lengthy development cycles, and the inherent inflexibility of conventional ASICs, and permit field design upgrades.

Features

- Very low cost, high-performance logic solution for high-volume, cost-conscious applications
- Dual-range V_{CCAUX} supply simplifies 3.3V-only design
- Suspend, Hibernate modes reduce system power
- Multi-voltage, multi-standard SelectIO™ interface pins
 - Up to 502 I/O pins or 227 differential signal pairs
 - LVCMOS, LVTTTL, HSTL, and SSTL single-ended I/O
 - 3.3V, 2.5V, 1.8V, 1.5V, and 1.2V signaling
 - Selectable output drive, up to 24 mA per pin
 - QUIETIO standard reduces I/O switching noise
 - Full 3.3V $\pm$ 10% compatibility and hot swap compliance

- 640+ Mb/s data transfer rate per differential I/O
- LVDS, RSDS, mini-LVDS, HSTL/SSTL differential I/O with integrated differential termination resistors
- Enhanced Double Data Rate (DDR) support
- DDR/DDR2 SDRAM support up to 400 Mb/s
- Fully compliant 32-/64-bit, 33/66 MHz PCI® technology support
- Abundant, flexible logic resources
 - Densities up to 25,344 logic cells, including optional shift register or distributed RAM support
 - Efficient wide multiplexers, wide logic
 - Fast look-ahead carry logic
 - Enhanced 18 x 18 multipliers with optional pipeline
 - IEEE 1149.1/1532 JTAG programming/debug port
- Hierarchical SelectRAM™ memory architecture
 - Up to 576 Kbits of fast block RAM with byte write enables for processor applications
 - Up to 176 Kbits of efficient distributed RAM
- Up to eight Digital Clock Managers (DCMs)
 - Clock skew elimination (delay locked loop)
 - Frequency synthesis, multiplication, division
 - High-resolution phase shifting
 - Wide frequency range (5 MHz to over 320 MHz)
- Eight low-skew global clock networks, eight additional clocks per half device, plus abundant low-skew routing
- Configuration interface to industry-standard PROMs
 - Low-cost, space-saving SPI serial Flash PROM
 - x8 or x8/x16 BPI parallel NOR Flash PROM
 - Low-cost Xilinx® Platform Flash with JTAG
 - Unique Device DNA identifier for design authentication
 - Load multiple bitstreams under FPGA control
 - Post-configuration CRC checking
- Complete Xilinx [ISE®](#) and [WebPACK™](#) development system software support plus [Spartan-3A Starter Kit](#)
- [MicroBlaze™](#) and [PicoBlaze™](#) embedded processors
- Low-cost QFP and BGA packaging, Pb-free options
 - Common footprints support easy density migration
 - Compatible with select [Spartan-3AN](#) nonvolatile FPGAs
 - Compatible with higher density [Spartan-3A DSP](#) FPGAs
- [XA Automotive](#) version available

Table 1: Summary of Spartan-3A FPGA Attributes

Device	System Gates	Equivalent Logic Cells	CLB Array (One CLB = Four Slices)				Distributed RAM bits ⁽¹⁾	Block RAM bits ⁽¹⁾	Dedicated Multipliers	DCMs	Maximum User I/O	Maximum Differential I/O Pairs
			Rows	Columns	CLBs	Slices						
XC3S50A	50K	1,584	16	12	176	704	11K	54K	3	2	144	64
XC3S200A	200K	4,032	32	16	448	1,792	28K	288K	16	4	248	112
XC3S400A	400K	8,064	40	24	896	3,584	56K	360K	20	4	311	142
XC3S700A	700K	13,248	48	32	1,472	5,888	92K	360K	20	8	372	165
XC3S1400A	1400K	25,344	72	40	2,816	11,264	176K	576K	32	8	502	227

Notes:

1. By convention, one Kb is equivalent to 1,024 bits.