Product Specification

(Preliminary)

Part Name: OLED Display Module

Part ID: LM130SB-128064

LI YUAN ELECTRONICS CO., LTD.

Notes:

1. Please contact Li Yuan Electronics Co., Ltd. before assigning your product based on this module specification.
2. The information contained herein is presented merely to indicate the characteristics and performance of our products. No responsibility is assumed by Li Yuan Electronics Co., Ltd.. For any intellectual property claims or other problems that may result from application baesd on the module described herein.

Revised History			
Part Number	REV	Revision Content	Revised
LM130SB-128064		First	20170928

Notce:

No part of this material may be reproduces or duplicated in any form or by any means without the written permission of Li Yuan Electronics Co., Ltd. . Li Yuan Electronics Co., Ltd. reserves the right to make changes to this material without notice. Li Yuan Electronics Co., Ltd. does not assume any liability of any kind arising out of any inaccuracies contained in this material or due to its application or use in any product or circuit ane, further, there is no representation that this material is applicable to products requiring high level reliability, such as, medical products. Moreover, no license to any intellectual property rights is granted by accordance with this material will be free from any patent or copyright infringement of a to strategic products under the control of Foreign Exchange and Foreign Trade Law of China and may require an export license from the Ministry of International Trade and Industry or other approval from another government agency.

Contents

1 Basic Specifications

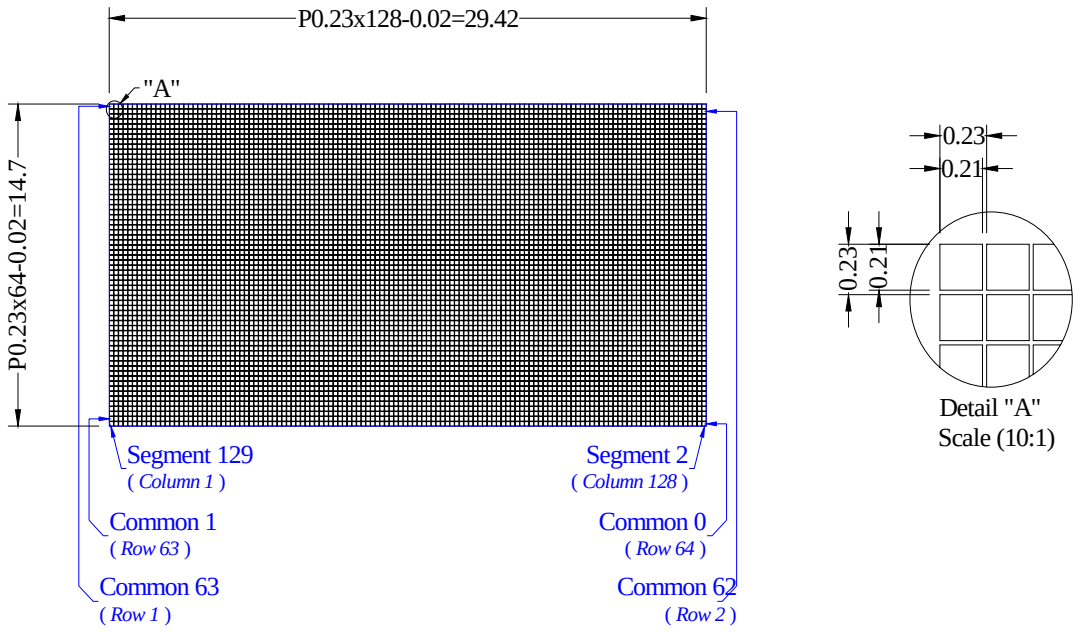
1.1 Display Specifications

Item	Specs
Display Mode	Passive Matrix OLED & Blue/White
Interface	3 wire SPI, 4 wire SPI, I2C
Drive Duty	1/64
Driver IC	SH1106
Shell	0.5T
Other	

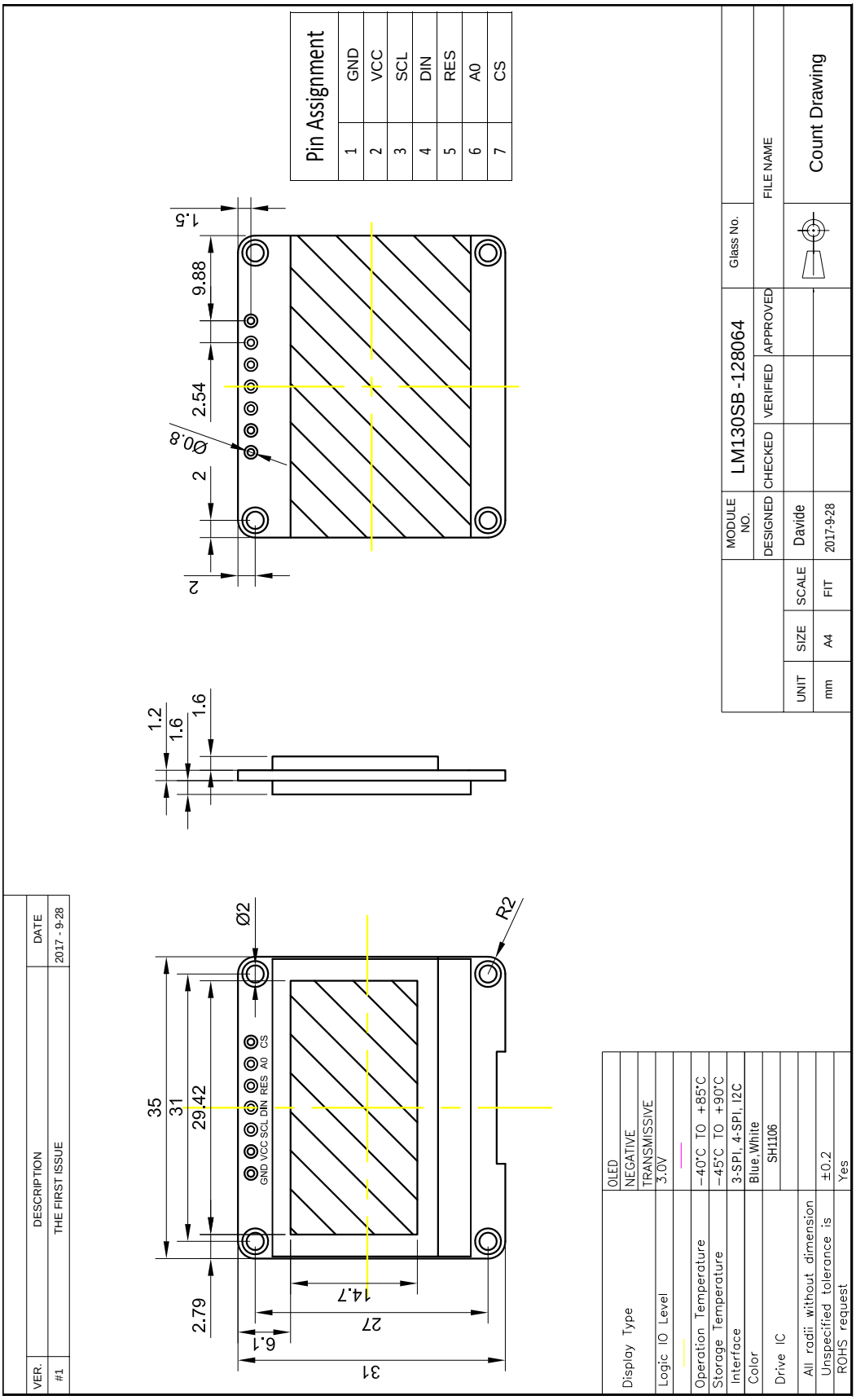
1.2 Mechanical Specifications

Item	Specs	Unit	Remark
Outline Drawing	35.0(W)x31.0(H)x4.4Max(T)	mm	
View Area	34.5(W)x23.0(H)	mm	
Active Area	29.42(W)x14.70(H)	mm	
Lattice	128dots x 64dots	--	
Pixel Pitch	0.23(W)x0.23(H)	mm	
Pixel Size	0.21(W)x0.21(H)	mm	

1.3 Active Area & Pixel Construction



1.4 Mechanical Drawing



1.5 Pin Definition

No.	Symbol	I/O	Function
1	GND	P	*Ground of Analog Circuit* This is an analog ground pin. It should be connected to VSS externally.
2	VCC	P	*Power Supply for Display Module Circuit* This is a voltage supply pin. It connected to external source.
3	SCL	I	*Serial Clock Input Signal* The transmission if information in the bus is following a clock signal. Each transmission of data bit is taken place during a single clock period of this pin.
4	DIN	I	*Serial Data Input Signal* This pin acts as a communication channel. The input data through DIN are latched at the rising edge of SCL in the sequence of MSB first and converted to 8-bit parallel data and handled at the rising edge of last serial clock.
5	RES	I	*Power Reset for Controller and Driver* This pin is reset signal input. When the pin is low, initialization of the chip is executed.
6	A0	I	*Data/Command Control* When the pin is pulled high and serial interface mode is selected, the data at DIN is treated as data. When it is pulled low, the data at DIN will be transferredto the command register. In I2C mode, this pin acts as SA0 for slave address selection.
7	CS	I	*Chip Select* This pin is the chip select input. The chip is enabled fo MCU communication only when CS is pulled low.

1.6 Interface Selection

MCU Interface Selection: IM0, IM1 on PCB board.
Pins Connected to MCU interface:D7~D0,R/W#, E/RD#, D/C#, CS#, RES#.

MCU Bus Interface Pin Selection

Pin Name	I^2C Interface	4-wire Serial interface	3-wire Serial interface
IM0	0	0	1
IM1	1	0	0

Note
(1) 0 is connected to V_{SS}
(2) 1 is connected to V_{DD}
(3) Default interface is 4-wire Serial interface.
(4) Please tell us the specific requirement of your company,we will provide appropriate interface to you.

The pin assignment at different interface mode is summarized in below table.

MCU interface assignment under different bus interface mode

Pin Name / Bus Interface	Control Signal		
	CS	A0	RES
3-wire SPI	CS	Tie LOW	RES
4-wire SPI	CS	A0	RES
I^2C	Tie LOW	A0	RES

2. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Notes
Power Supply Voltage	VCC	2	6	V	1,2
Power Supply Current	Icc	-	18	mA	1,2
Operating Temperature	Top	-30	70	℃	-
Storage Temperature	Tstg	-40	80	℃	-

Note 1: All the above voltage are on the basis of "GND=0V".

Note 2: When this module is used beyond the above absolute maximum Ratings, permanent breakage of the module may occur. Also, for normal operations, it is desirable to use this module under the conditions according to Section 3. "Electrical Characteristics". If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate.

3.Electrical Characteristics

3.1 DC Charateristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage	VCC	Ta=25℃	2.5	-	5.5	V
High Level Input	VIH	Iout=100uA 3.3MHz	1.32	-	3.6	V
Low Level Input	VIL	Iout=100uA 3.3MHz	0	-	0.7	V
Supply Current	Icc	Note1	-	25	30	mA
		Note2	-	45	50	mA
Sleep Mode Current	Icc, Sleep		-	2	10	uA

Note1: VCC=3.3V, 50% Display Area Turn on;

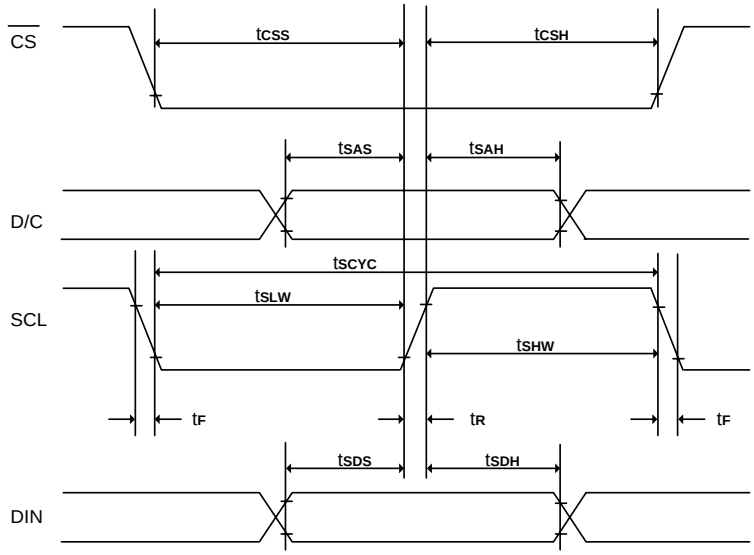
Note2: VCC=3.3V, 100% Display Area Turn on.

3.2 Optics & Electrical Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Brightness	Lbr	With Polarizer (Note 3)	110	130	-	Cd/m2
C.I.E.(White)	(X) (Y)	With Polarizer	0.28 0.29	0.32 0.33	0.36 0.37	
C.I.E.(Blue)	(X) (Y)	With Polarizer	0.12 0.22	0.16 0.26	0.20 0.30	
Dark Room Contrast	CR		-	>2000:1	-	
View Angle			>160	-	-	degree

3.3 AC Characteristics

3.3.1 Serial Interface Timing Characteristics: (4-wire SPI)

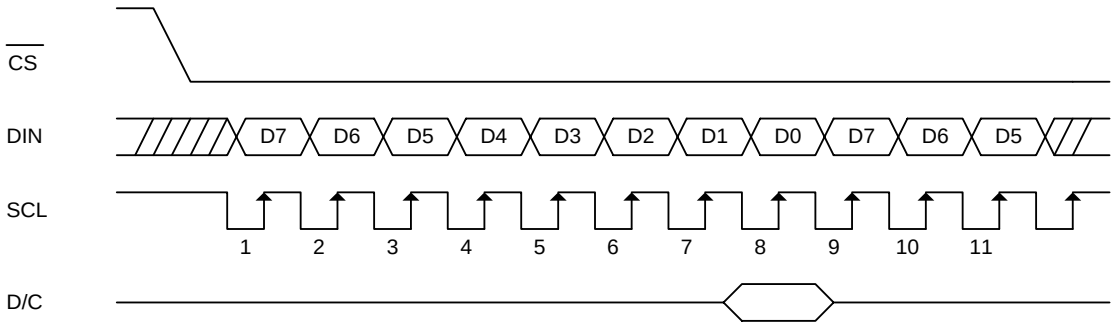


(Vcc = 1.65 - 3.5V, TA = +25°C)

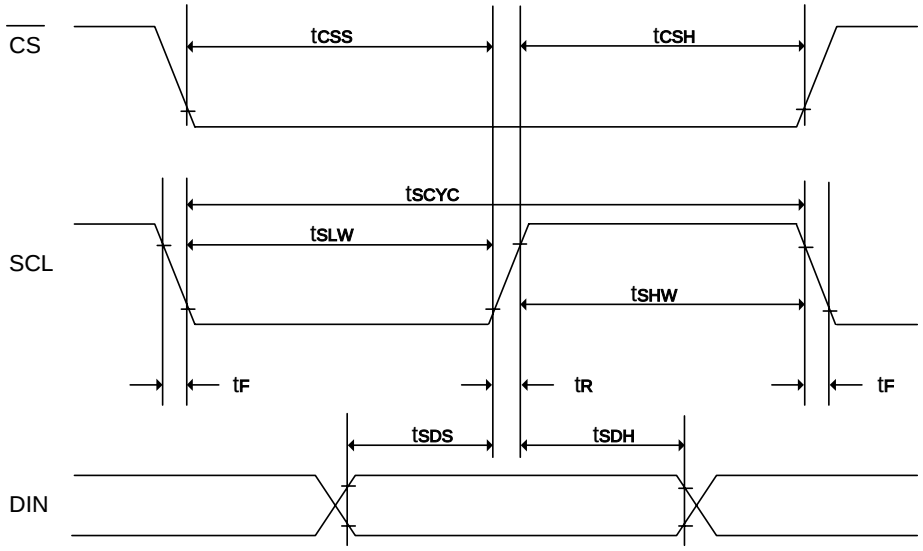
Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
tSCYC	Serial clock cycle	500	-	-	ns	
tSAS	Address setup time	300	-	-	ns	
tSAH	Address hold time	300	-	-	ns	
tSDS	Data setup time	200	-	-	ns	
tSDH	Data hold time	200	-	-	ns	
tCSS	$\overline{CS}$ setup time	240	-	-	ns	
tCSH	$\overline{CS}$ hold time time	120	-	-	ns	
tSHW	Serial clock H pulse width	200	-	-	ns	
tSLW	Serial clock L pulse width	200	-	-	ns	
tR	Rise time	-	-	30	ns	
tF	Fall time	-	-	30	ns	

(Vcc = 2.4 - 3.5V, TA = +25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
tSCYC	Serial clock cycle	250	-	-	ns	
tSAS	Address setup time	150	-	-	ns	
tSAH	Address hold time	150	-	-	ns	
tSDS	Data setup time	100	-	-	ns	
tSDH	Data hold time	100	-	-	ns	
tCSS	$\overline{CS}$ setup time	120	-	-	ns	
tCSH	$\overline{CS}$ hold time time	60	-	-	ns	
tSHW	Serial clock H pulse width	100	-	-	ns	
tSLW	Serial clock L pulse width	100	-	-	ns	
tR	Rise time	-	-	15	ns	
tF	Fall time	-	-	15	ns	



3.3.2 Serial Interface Timing Characteristics: (3-wire SPI)

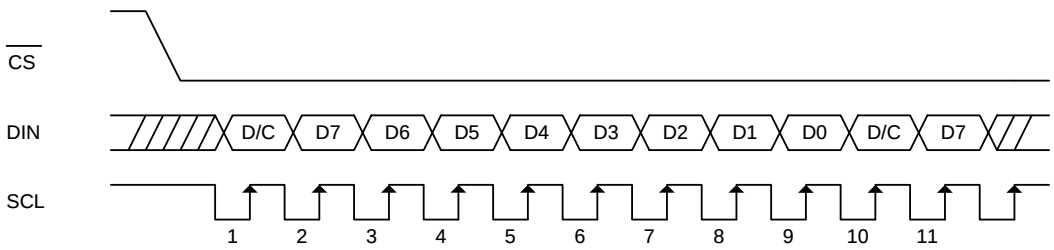


(Vcc = 1.65 - 3.5V, TA = +25°C)

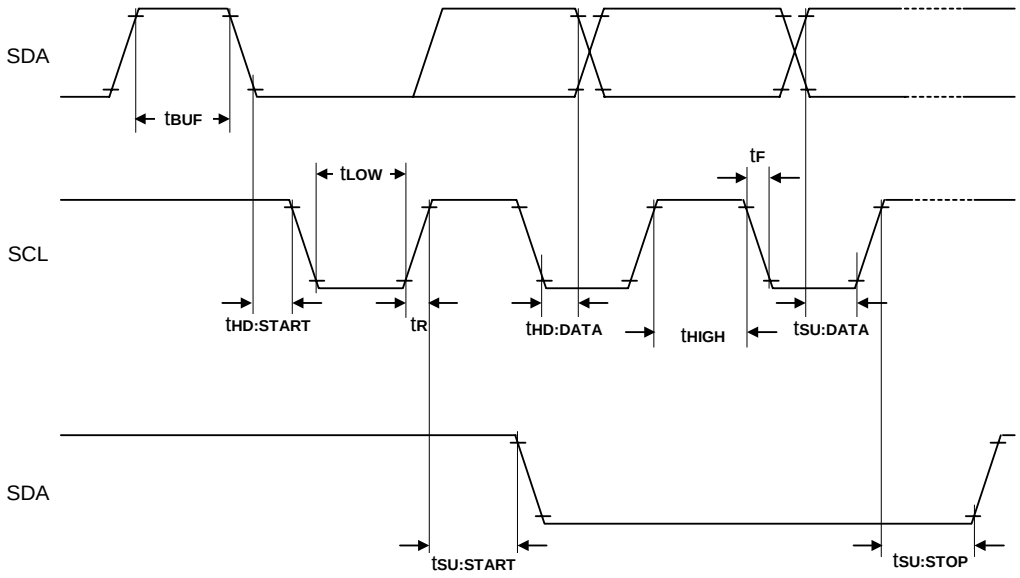
Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
tSCYC	Serial clock cycle	500	-	-	ns	
tSDS	Data setup time	200	-	-	ns	
tSDH	Data hold time	200	-	-	ns	
tCSS	$\overline{CS}$ setup time	240	-	-	ns	
tCSH	$\overline{CS}$ hold time time	120	-	-	ns	
tSHW	Serial clock H pulse width	200	-	-	ns	
tSLW	Serial clock L pulse width	200	-	-	ns	
tR	Rise time	-	-	30	ns	
tF	Fall time	-	-	30	ns	

(Vcc = 2.4 - 3.5V, TA = +25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
tSCYC	Serial clock cycle	250	-	-	ns	
tSDS	Data setup time	100	-	-	ns	
tSDH	Data hold time	100	-	-	ns	
tCSS	$\overline{CS}$ setup time	120	-	-	ns	
tCSH	$\overline{CS}$ hold time time	60	-	-	ns	
tSHW	Serial clock H pulse width	100	-	-	ns	
tSLW	Serial clock L pulse width	100	-	-	ns	
tR	Rise time	-	-	15	ns	
tF	Fall time	-	-	15	ns	



3.3.3 I2C Interface Timing Characteristics:



(Vcc = 1.65 - 3.5V, TA = +25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
fSCL	SCL clock frequency	DC	-	400	kHz	
TLOW	SCL clock Low pulse width	1.3	-	-	uS	
THIGH	SCL clock H pulse width	0.6	-	-	uS	
TSU:DATA	data setup time	100	-	-	nS	
THD:DATA	data hold time	0	-	0.9	uS	
TR	SCL, SDA rise time	20+0.1Cb	-	300	nS	
TF	SCL, SDA fall time	20+0.1Cb	-	300	nS	
Cb	Capacity load on each bus line	-	-	400	pF	
TSU:START	Setup timefor re-START	0.6	-	-	uS	
THD:START	START Hold time	0.6	-	-	uS	
TSU:STOP	Setup time for STOP	0.6	-	-	uS	
TBUF	Bus free times between STOP and START condition	1.3	-	-	uS	

4 Functional Specificaton

4.1 MCU Serial Interface (4-wire SPI)

The 4-wire serial interface consists of serial clock: SCL, serial data:SDIN, A0, CS.

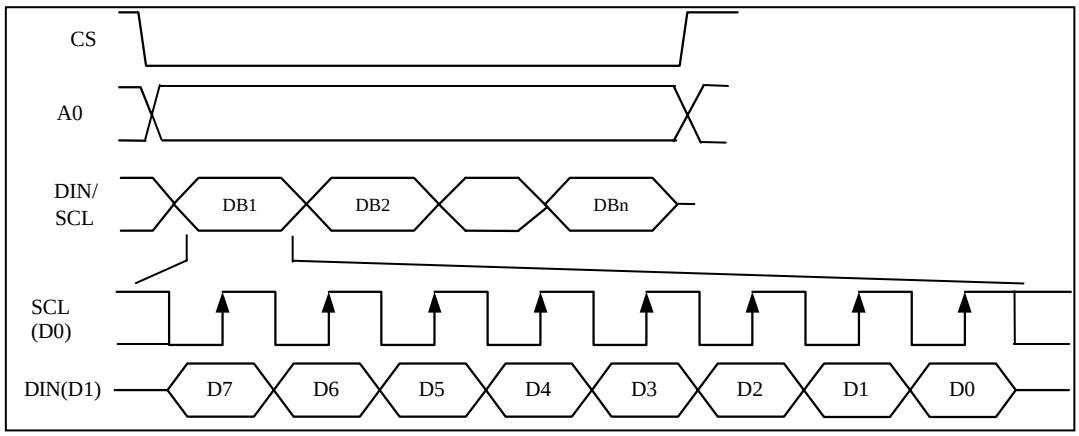
Control pins of 4-wire Serial interface

Functio	CS	A0	SCL
Write command	L	L	↑
Write data	L	H	↑

Note
(1) H stands for HIGH in signal
(2) L stands for LOW in signal

DIN is shifted into an 8-bit shift register on every rising edge of SCL in the order of D7, D6, ... D0. A0 is sampled on every eighth clock and the data byte in the shift register is written to the Graphic Display Data RAM (GDDRAM) or command register in the same clock. Under serial mode, only write operations are allowed.

Write procedure in 4-wire Serial interface mode



4.2 MCU Serial Interface (3-wire SPI)

The 3-wire serial interface consists of serial clock: SCLK, serial data: SDIN, and CS#. In 3-wire SPI mode, A0 can be connected

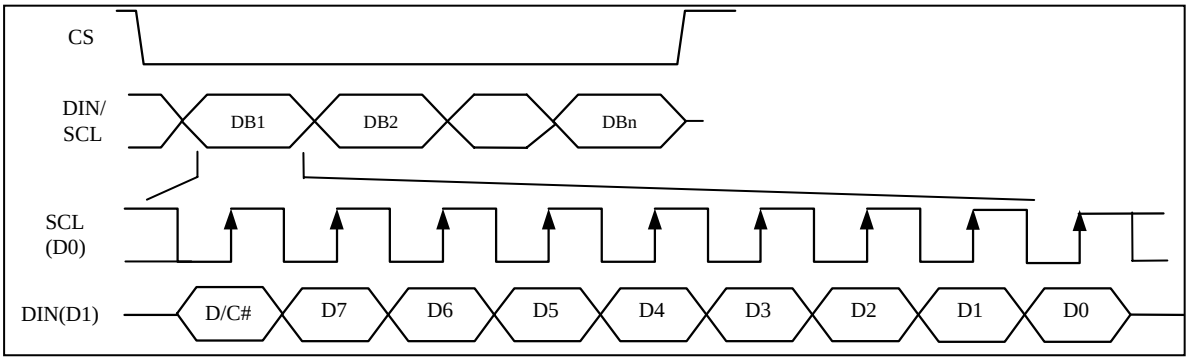
The operation is similar to 4-wire serial interface while A0 pin is not used. There are altogether 9-bits will be shifted into the shift register on every ninth clock in sequence: A0 bit, D7 to D0 bit. The A0 bit (first bit of the sequential data) will determine the following data byte in the shift register is written to the display Data RAM (A0 bit=1) or the command register (A0 bit = 0). Under serial mode, only write operation are allowed.

Control pins of 3-wire Serial interface

Functio	CS	A0	SCL
Write command	L	Tie LOW	↑
Write data	L	Tie LOW	↑

Note
(1) L stands for LOW in signal

Write procedure in 3-wire Serial interface mode



4.3 MCU I2C Interface

The I2C communication interface consists of slave address bit SA0, I2C-bus data signal SDA(SDAOUT/D2 for output and SDAIN/D1 for input) and I2C-bus clock signal SCL (D0). Both the data and clock signals must be connected to pull-up resistors. /RES is used for the initialization of device.

a) Slave address bit (SA0)

SSD1306 has to recognize the slave address before transmitting or receiving any information by the I2C-bus. The device will respond to the slave address following by the slave address bit("SA0" bit) and the read/write select bit ("R/W#" bit) with the following byte format,

b7	b6	b5	b4	b3	b2	b1	b0
0	1	1	1	1	0	SA0	R/W

"SA0" bit provides an extension bit for the slave address. Either "0111100" or "0111101", can be selected as the slave address of SSD1306. DC pin acts as SA0 for slave address selection. "R/W" bit is used to determine the operation mode of the I2C-bus interface. R/W=1, it is in read mode. R/W=0, it is in write mode.

b) I2C-bus data signal (SDA) SDA acts as a communication channel between the transmitter and the receiver. The data and the acknowledgement are sent through the SDA.

It should be noticed that the ITO track resistance and the pulled-up resistance at "SDA" pin becomes a voltage potential divider. As a result, the acknowledgement would not be possible to attain a valid logic 0 level in "SDA". "SDAIN" and "SDAOUT" are tied together and serve as SDA. The "SDAIN" pin must be connected to act as SDA. The "SDAOUT" pin may be disconnected. When "SDAOUT" pin is disconnected, the acknowledgement signal will be ignored in the I2C-bus.

b) I2C-bus clock signal (SCL)

The transmission of information in the I2C-bus is following a clock signal, SCL. Each transmission of data bit is taken place during a single clock period of SCL.

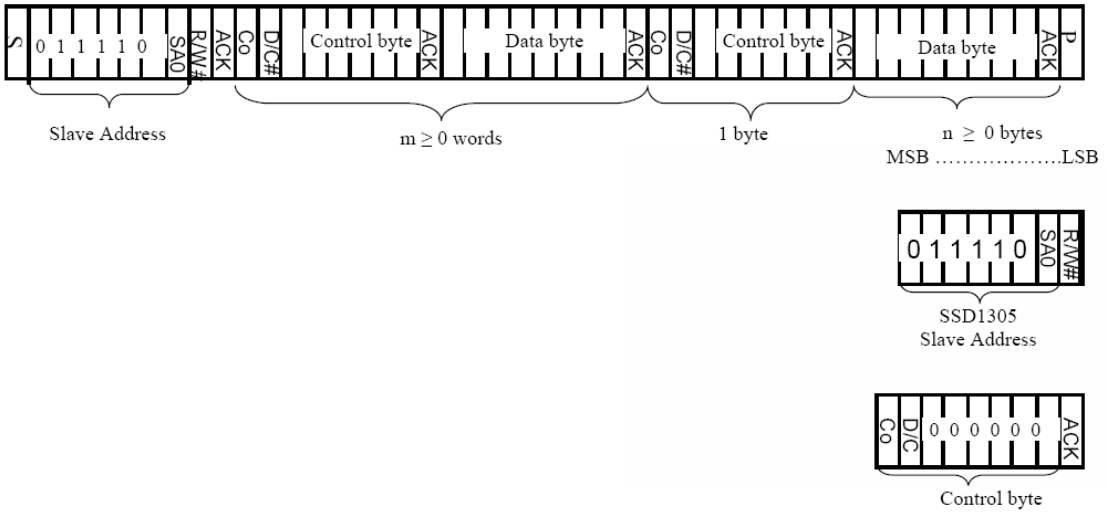
4.3.1 I2C-bus Write data

The I2C-bus interface gives access to write data and command into the device. Please refer to the following Figure for the write mode of I2C-bus in chronological order.

I2C-bus data format

Note: Co – Continuation bit
D/C# - Data / Command Selection bit
ACK – Acknowledgement
SA0 – Slave address bit
R/W# - Read/Write Selection bit
S – Start Condition / P – Stop Condition

Write mode



4.3.2 Write mode for I2C

1) The master device initiates the data communication by a start condition. The definition of the start condition is shown in the followng Figure (1). The start condition is established by pulling the SDA from HIGH to LOW while the SCL stays HIGH.

2) The slave address is following the start condition for recognition use. For the SSD1306, the slave address is either “b0111100” or “b0111101” by changing the SA0 to LOW or HIGH (DC pin acts as SA0).

3) The write mode is established by setting the R/W bit to logic “0”.

4) An acknowledgement signal will be generated after receiving one byte of data,including the slave address and the R/W bit. Please refer to the following Figure (2) for the graphical representation of the acknowledge signal. The acknowledge bit is defined as the SDA line is pulled down during the HIGH period of the acknowledgement related clock pulse.

5) After the transmission of the slave address, either the control byte or the data byte may be sent across the SDA. A control byte mainly consists of Co and A0 bits following by six “0” ‘s.

a. If the Co bit is set as logic “0”, the transmission of the following information will contain data bytes only.

b. The A0 bit determines the next data byte is acted as a command or a data. If the A0 bit is set to logic "0", it defines the following data byte as a command. If the A0 bit is set to logic "1", it defines the following data byte as a data which will be stored at the GDDRAM. The GDDRAM column address pointer will be increased by one automatically after each data write.

6) Acknowledge bit will be generated after receiving each control byte or data byte.

7) The write mode will be finished when a stop condition is applied. The stop condition is also defined in Figure (1). The stop condition is established by pulling the "SDA in" from LOW to HIGH while the "SCL" stays HIGH.

Figure (1): Definition of the Start and Stop Condition

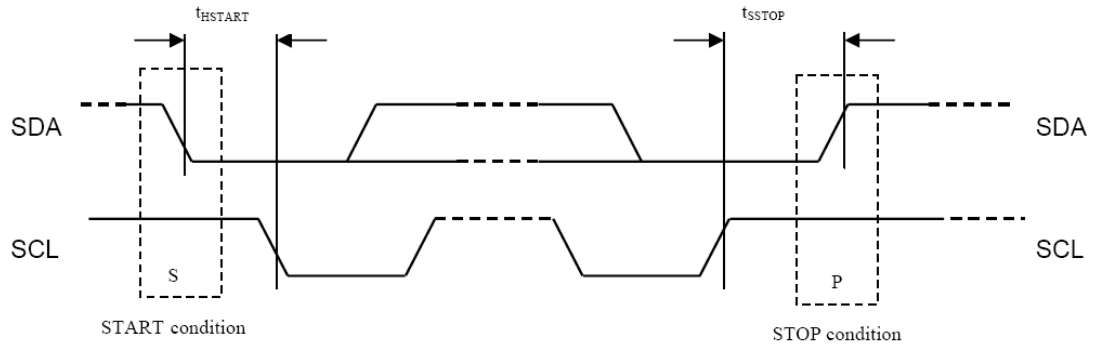
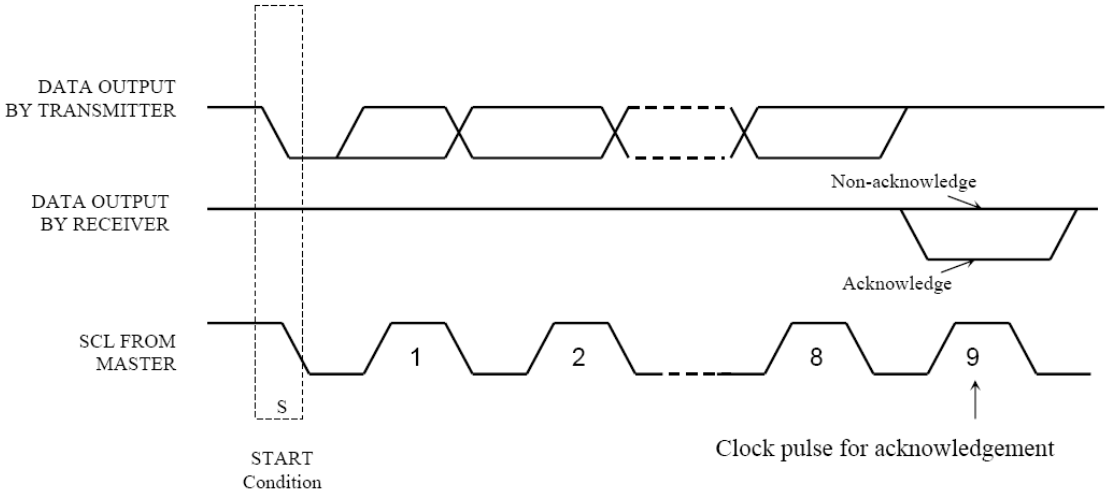


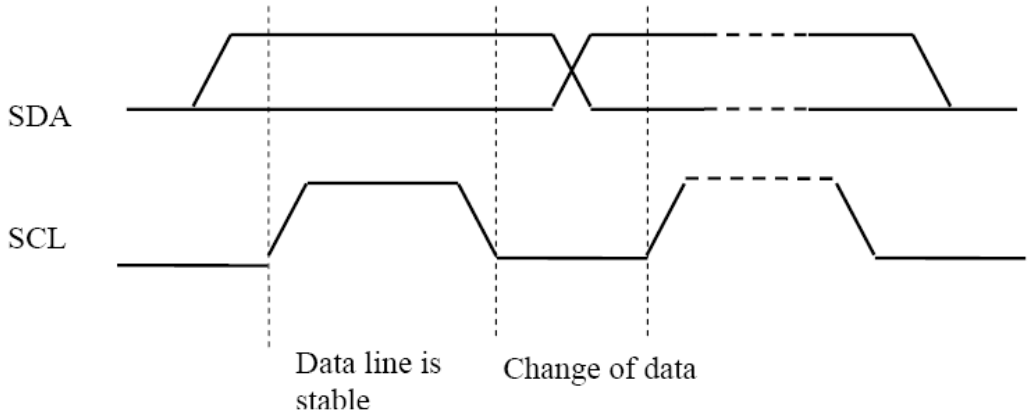
Figure (2):Definition of the acknowledgement condition



Please be noted that the transmission of the data bit has some limitations.

1. The data bit, which is transmitted during each SCL pulse, must keep at a stable state within the "HIGH" period of the clock pulse. Please refer to the Figure (3) for graphical representations.Except in start or stop conditions, the data line can be switched only when the SCL is LOW.
2. Both the data line (SDA) and the clock line (SCL) should be pulled up by external resistors.

Figure (3):Definition of the data transfer condition



4.6 Command Decoder

Refe to the Technical Manual for the SH1106.

4.7 FR synchronization

Refer to the Technical Manual for the SH1106.

4.8 Reset Circuit

When /RES input is low, the chip is initialized with the following status:

1. Display is OFF.
2. 128x64 MUX Display Mode.
3. Normal segment and display data column address and row address mapping (SEG0 mapped to address 00h and COM0 mapped to address 00h).
4. Shift register data clear in serial interface.
5. Display start line is set at display RAM address 0.
6. Column address counter is set at 0.
7. Normal scan direction of the COM outputs.
8. Contrast control register is set at 7Fh.
9. Normal display mode (Equivalent to A4h command).

5. Reliability

5.1 Contents of Reliability Tests

Item	Conditions		Criteria
High Temperature Operation	85℃	TBD	The operational Functions work
Low Temperature Operation	-40℃	TBD	
High Temperature Storage	90℃	TBD	
Low Temperature Storage	-45℃	TBD	
High Temperature/Humidity Operation	60℃	TBD	
Thermal Shock	-40℃⇔90℃	TBD	

* The samples used for the above tests do not include polarizer.
* No moisture condensation is observed during tests.

5.2 Life time

End of lifetime is specified as 50% of initial brightness.

Parameter	Min	Max	Unit	Condition	Notes
Operating Life Time	50,000	-	Hrs	80 cd/m2,50%checkerboard	6
Storage Life Time	200,000	-	Hrs	Ta=25 ℃,50%RH	-

Note 6: The average operating lifetime at room temperature is estimated by the accelerated operation at high temperature conditions.

5.3 Failure Check Standard

After the completion of the described reliability test, the samples were left at room temperature for 2 hrs prior to conducting the failure test at 23+/-5℃; 55+/-15%RH.

6. Outgoing Quality Control Specifications

6.1 Environment Required

Customer's test & measurement are required to be conducted under the following conditions:

Temperature:	23+/-5℃
Humidity:	55+/-15%RH
Fluorescent Lamp:	30W
Distance between the Panel & Lamp:	>=50 cm
Distance between the Panel & Eyes of the Inspector	>=30 cm

Finger glove (or finger cover) must be worn by the inspector.

Inspection table or jig must be anti-electrostatic.

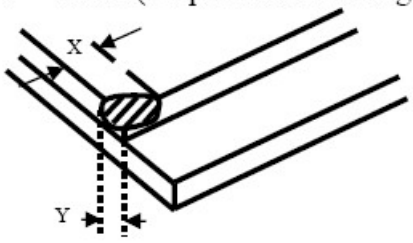
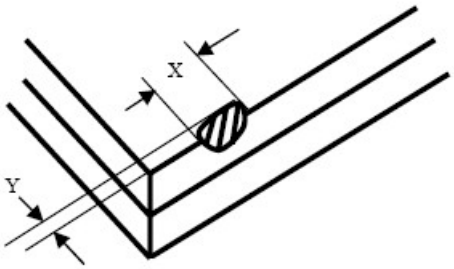
6.2 Sampling Plan

Level II, Normal Inspection, Single Sampling,MIL-STD-105E

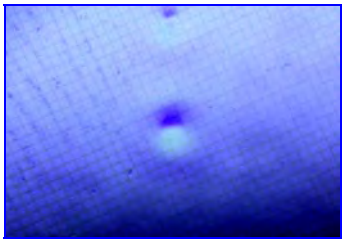
6.3 Criteria & Acceptable Quality Level

Partition	AQL	Definition
Major	0.65	DefectsinPatternCheck(DisplayOn)
Minor	1.0	Defects in Cosmetic Check (Display Off)

6.3.1 Cosmetic Check (Display Off) in Non-Active Area

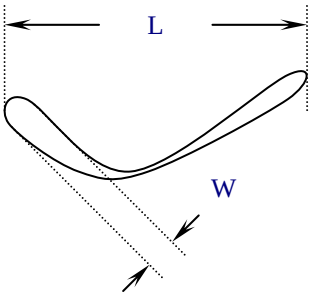
Check Item	Classification	Criteria
Panel General Chipping	Minor	X > 6 mm (Along with Edge) Y > 1 mm (Perpendicular to edge)  

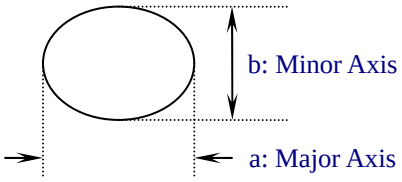
6.3.2 Cosmetic Check (Display Off) in Active Area

Check Item	Classification	Criteria
Any Dirt & Scratch on Polarizer's Protective Film	Acceptable	Ignore for not Affect the Polarizer
Scratches, Fiber, Line-Shape Defect (On Polarizer)	Minor	W ≤ 0.1 Ignore W > 0.1, L ≤ 2 n ≤ 1 L > 2 n = 0
Dirt, Black Spot, Foreign Material, (On Polarizer)	Minor	Φ ≤ 0.1 Ignore 0.1 <Φ ≤ 0.25 n ≤ 1 0.25 <Φ n = 0
Dent, Bubbles, White spot (Any Transparent Spot on Polarizer)	Minor	Φ ≤ 0.5 ➔ Ignore if no Influence on Display 0.5 < Φ n = 0 
Fingerprint, Flow Mark (On Polarizer)	Minor	Not Allowable

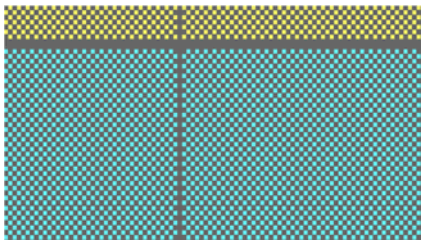
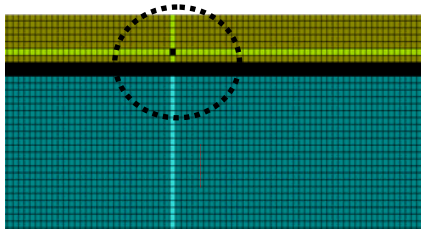
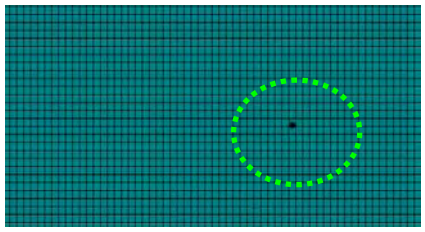
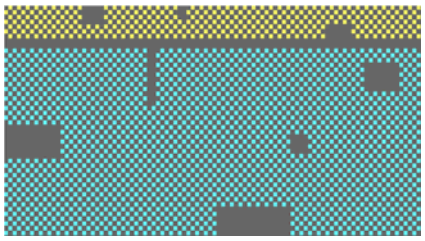
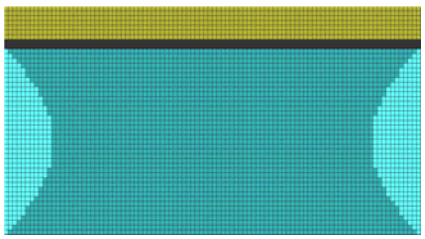
* Protective film should not be tear off when cosmetic check.

** Definition of W & L & Φ (Unit: mm): Φ = (a + b) / 2





6.3.3 Pattern Check (Display On) in Active Area

Check Item	Classification	Criteria
No Display	Major	
Flicker	Major	Not Allowable
Missing Line	Major	
Pixel Short	Major	
Darker Pixel	Major	
Wrong Display	Major	
Un-uniform	Major	

7. Precautions When Using These OLED Display Modules

7.1 Handling Precautions

1) Since the display panel is being made of glass, do not apply mechanical impacts such us dropping from a high position.
2) If the display panel is broken by some accident and the internal organic substance leaks out, be careful not to inhale nor lick the organic substance.
3) If pressure is applied to the display surface or its neighborhood of the OLED display module, the cell structure may be damaged and be careful not to apply pressure to these sections.
4) The polarizer covering the surface of the OLED display module is soft and easily scratched. Please be careful when handling the OLED display module.
5) When the surface of the polarizer of the OLED display module has soil,clean the surface. It takes advantage of by using following adhesion tape.
   * Scotch Mending Tape No. 810 or an equivalent

   Never try to breathe upon the soiled surface nor wipe the surface using cloth containing solvent such as ethyl alcohol, since the surface of the polarizer will become cloudy.

   Also, pay attention that the following liquid and solvent may spoil the polarizer
   * Water
   * Ketone
   * Aromatic Solvents
6) When installing the OLED display module, be careful not to apply twisting stress or deflection stress to the OLED display module. And, do not over bend the film with electrode pattern layouts. These stresses will influence the display performance. Also, secure sufficient rigidity for the outer cases.
7) Do not apply stress to the LSI chips and the surrounding molded sections.
8) Do not disassemble nor modify the OLED display module.
9) Do not apply input signals while the logic power is off.
10) Pay sufficient attention to the working environments when handing OLED display modules to prevent occurrence of element breakage accidents by static electricity.
    * Be sure to make human body grounding when handling OLED display modules.
    * Be sure to ground tools to use or assembly such as soldering irons.
    * To suppress generation of static electricity, avoid carrying out assembly work under dry environments.
    * Protective film is being applied to the surface of the display panel of the OLED display module. Be careful since static electricity may be generated when exfoliating the protective film.
11) Protection film is being applied to the surface of the display panel and removes the protection film before assembling it. At this time, if the OLED display module has been stored for a long period of time, residue adhesive material of the protection film may remain on the surface of the display

panel after removed of the film. In such case, remove the residue material by the method introduced in the above Section 5).

12) If electric current is applied when the OLED display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful to avoid the above.

7.2 Storage Precautions

1) When storing OLED display modules, put them in static electricity preventive bags avoiding exposure to direct sun light nor to lights of fluorescent lamps.and, also, avoiding high temperature and high humidity environment or low temperature (less than 0° C) environments. (We recommend you to store these modules in the packaged state when they were shipped from Li Yuan Electronics Co.,Ltd.)
   At that time, be careful not to let water drops adhere to the packages or bags nor let dewing occur with them.
2) If electric current is applied when water drops are adhering to the surface of the OLED display module, when the OLED display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful about the above.

7.3 Designing Precautions

1) The absolute maximum ratings are the ratings which cannot be exceeded for OLED display module, and if these values are exceeded, panel damage may be happen.
2) To prevent occurrence of malfunctioning by noise, pay attention to satisfy the VIL and VIH specifications and, at the same time, to make the signal line cable as short as possible.
3) We recommend you to install excess current preventive unit (fuses, etc.) to the power circuit (VDD). (Recommend value: 0.5A)
4) Pay sufficient attention to avoid occurrence of mutual noise interference with the neighboring devices.
5) As for EMI, take necessary measures on the equipment side basically.
6) When fastening the OLED display module, fasten the external plastic housing section.
7) If power supply to the OLED display module is forcibly shut down by such errors as taking out the main battery while the OLED display panel is in operation, we cannot guarantee the quality of this OLED display module.
8) The electric potential to be connected to the rear face of the IC chip should beasfollows:SH1106.
   * Connection (contact) to any other potential than the above may lead to rupture of the IC.

7.4 Precautions when disposing of the OLED display modules

1) Request the qualified companies to handle industrial wastes when disposing of the OLED display modules. Or, when burning them, be sure to observe the environmental and hygienic laws and regulations.

7.5 Other Precautions

1) When an OLED display module is operated for a long of time with fixed pattern may remain as an after image or slight contrast deviation may occur. Nonetheless, if the operation is interrupted and left unused for a while, normal state can be restored. Also, there will be no problem in the reliability of the module.

2) To protect OLED display modules from performance drops by static electricity rapture, etc., do not touch the following sections whenever possible while handling the OLED display modules.

* Pins and electrodes

*Patternlayoutssuchasthe FPC

3) With this OLED display module, the OLED driver is being exposed. Generally speaking, semiconductor elements change their characteristics when light is radiated according to the principle of the solar battery. Consequently, if this OLED driver is exposed to light, malfunctioning may occur.

* Design the product and installation method so that the OLED driver may be shielded from light in actual usage.

* Design the product and installation method so that the OLED driver may be shielded from light during the inspection processes.

4) Although this OLED display module stores the operation state data by the commands and the indication data, when excessive external noise, etc. enters into the module, the internal status may be changed. It therefore is necessary to take appropriate measures to suppress noise generation or to protect from influences of noise on the system design.

5) We recommend you to construct its software to make periodical refreshment of the operation statuses (re-setting of the commands and re-transference of the display data) to cope with catastrophic noise.

8. Appendixes

8.1 Display-module Software Initial Setting

```
Write_Command(0xAE);   //display off
Write_Command(0x20);   //Set Memory Addressing Mode<00FF>
Write_Command(0x10);   //Addressing Modee
Write_Command(0xb0);   //Set Page Start Address for Page Addressing Mode,0-7
Write_Command(0xc8);   //Set COM Output Scan Direction
Write_Command(0x02);   //---set low column address
Write_Command(0x10);   //---set high column address
Write_Command(0x40);   //--set start line address
Write_Command(0x81);   //--set contrast control register
Write_Command(0xaf);
Write_Command(0xa1);   //--set segment re-map 0 to 127
Write_Command(0xa6);   //--set normal display
Write_Command(0xa8);   //--set multiplex ratio(1 to 64)
Write_Command(0x3F);
Write_Command(0xa4);   //0xa4,Output follows RAM content;0xa5,Output ignores RAM content
Write_Command(0xd3);   //-set display offset
Write_Command(0x00);   //-not offset
Write_Command(0xd5);   //--set display clock divide ratio/oscillator frequency
Write_Command(0xf0);   //--set divide ratio
Write_Command(0xd9);   //--set pre-charge period
Write_Command(0x22);
Write_Command(0xda);   //--set com pins hardware configuration
Write_Command(0x12);
Write_Command(0xdb);   //--set vcomh
Write_Command(0x20);   //0x20,0.77xVcc
Write_Command(0x8d);   //--set DC-DC enable
Write_Command(0x14);
Write_Command(0xaf);   //--turn on oled panel
```