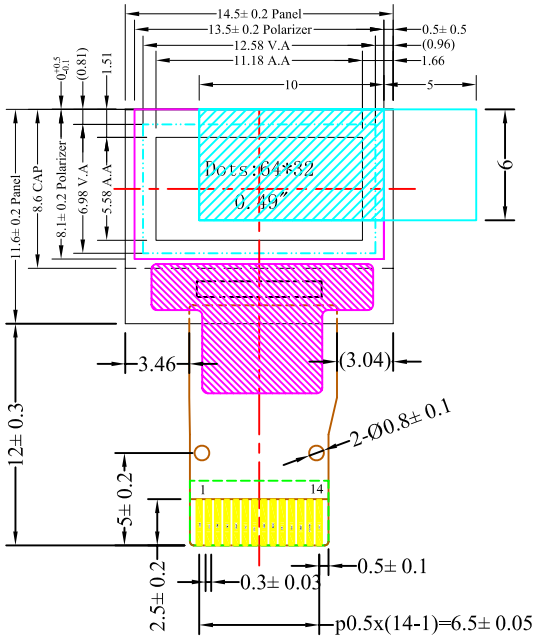
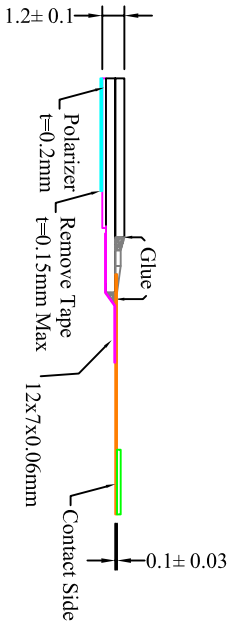
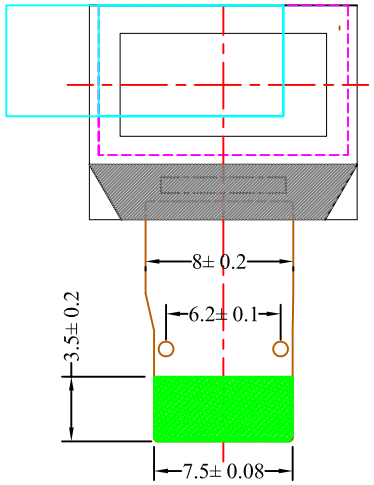
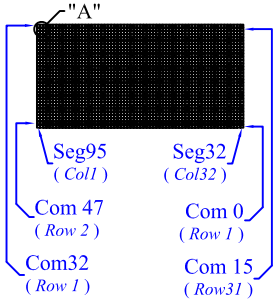
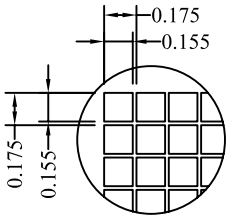










Detail "A"
Scale (10:1)

Pin	Symbol
1	C2P
2	C2N
3	C1P
4	C1N
5	VBAT
6	NC
7	VSS
8	VDD
9	RES#
10	SCL
11	SDA
12	IREF
13	VCOMH
14	VCC

Notes:

1. Color: White
2. Driver IC: SH1116
3. FPC Number: TBD
4. Interface: IIC
5. General Tolerance: ± 0.30

1.5 Pin Definition

Pin Number	Symbol	I/O	Function
Power Supply			
8	VDD	P	**Power Supply for Logic** This is a voltage supply pin. It must be connected to external source.
7	VSS	P	**Ground of Logic Circuit** This is a ground pin. It acts as a reference for the logic pins. It must be connected to external ground.
14	VCC	P	**Power Supply for OEL Panel** This is the most positive voltage supply pin of the chip. A stabilization capacitor should be connected between this pin and V_{SS} when the converter is used. It must be connected to external source when the converter is not used.
Driver			
12	IREF	I	**Current Reference for Brightness Adjustment** This pin is segment current reference pin. A resistor should be connected between this pin and V_{SS}. Set the current at 12.5μA maximum.
13	VCOMH	O	**Voltage Output High Level for COM Signal** This pin is the input pin for the voltage output high level for COM signals. A capacitor should be connected between this pin and V_{SS}.
DC/DC Converter			
5	VBAT	P	**Power Supply for DC/DC Converter Circuit** This is the power supply pin for the internal buffer of the DC/DC voltage converter. It must be connected to external source when the converter is used. It should be connected to V_{DD} when the converter is not used.
3 / 4 1 / 2	C1P / C1N C2P / C2N	I	**Positive Terminal of the Flying Inverting Capacitor** **Negative Terminal of the Flying Boost Capacitor** The charge-pump capacitors are required between the terminals. They must be floated when the converter is not used.
Interface			
9	RES#	I	**Power Reset for Controller and Driver** This pin is reset signal input. When the pin is low, initialization of the chip is executed. Keep this pin pull high during normal operation.

1.5 Pin Definition (Continued)

Pin Number	Symbol	I/O	Function
Interface (Continued)			
10	SCL	I	**IIC Bus Clock Signal** The transmission if information in the I2C bus is following a clock sigmal. Each transmission of data bit is taken place during a single clock period of this pin.
11	SDA	I/O	**I2C Bus Data Signal** This pin acts as a communication channel between the transmitter and the receiver.
Reserve			
6	VBREF	-	NC

2. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Notes
Supply Voltage for Logic	V_{DD}	-0.3	4	V	1, 2
Supply Voltage for Display	V_{CC}	0	16	V	1, 2
Supply Voltage for DC/DC (Internal DC/DC Enable)	*V_{bat}*	*-0.3*	*4.3*	*V*	*1, 2*
Operating Temperature	T_{OP}	-40	85	°C	
Storage Temperature	T_{STG}	-40	85	°C	3
Life Time (120 cd/m^2)		10,000	-	hour	4
Life Time (80 cd/m^2)		30,000	-	hour	4
Life Time (60 cd/m^2)		50,000	-	hour	4

Note 1: All the above voltages are on the basis of "V_{SS} = 0V".

Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. Also, for normal operations, it is desirable to use this module under the conditions according to Section 3. "Optics & Electrical Characteristics". If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate.

Note 3: The defined temperature ranges do not include the polarizer. The maximum withstood temperature of the polarizer should be 80°C.

Note 4: V_{CC} = 7.25V, T_a = 25°C, 50% Checkerboard.
Software configuration follows Section 4.4 Initialization.
End of lifetime is specified as 50% of initial brightness reached. The average operating lifetime at room temperature is estimated by the accelerated operation at high temperature conditions.

3. Optics & Electrical Characteristics

3.1 Optics Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Brightness (V_{CC} Supplied Externally)	L_{br}	Note 5	160	-	-	cd/m^2
Brightness (V_{CC} Generated by Internal DC/DC)	*L_{br}*	*Note 6*	*160*	*180*	-	*cd/m^2*
C.I.E. (White)	(x) (y)	C.I.E. 1931	0.28 0.31	0.32 0.35	0.36 0.39	
Dark Room Contrast	CR		-	2000:1	-	
Viewing Angle			-	Free	-	degree

* Optical measurement taken at V_{DD} = 2.8V, V_{CC} = 7.25V.
Software configuration follows Section 4.4 Initialization.

3.2 DC Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage for Logic	V_{DD}		1.65	2.8	3.3	V
Supply Voltage for Display (Supplied Externally)	V_{CC}	Note 5 (Internal DC/DC Disable)	7	-	9.0	V
Supply Voltage for DC/DC	*V_{BAT}*	*Internal DC/DC Enable*	*3.5*	*-*	*4.2*	*V*
Supply Voltage for Display (Generated by Internal DC/DC)	*V_{CC}*	*Note 6 (Internal DC/DC Enable)*	7	7.25	7.5	*V*
High Level Input	V_{IH}	I_{OUT} = 100μA, 3.3MHz	$0.8\times V_{DD}$	-	V_{DD}	V
Low Level Input	V_{IL}	I_{OUT} = 100μA, 3.3MHz	0	-	$0.2\times V_{DD}$	V
High Level Output	V_{OH}	I_{OUT} = 100μA, 3.3MHz	$0.9\times V_{DD}$	-	V_{DD}	V
Low Level Output	V_{OL}	I_{OUT} = 100μA, 3.3MHz	0	-	$0.1\times V_{DD}$	V
Operating Current for V_{DD}	I_{DD}		-	180	300	μA
Operating Current for V_{CC} (V_{CC} Supplied Externally)	I_{CC}	Note 7	-	5	10	mA
Operating Current for V_{BAT} (V_{CC} Generated by Internal DC/DC)	*I_{BAT}*	*Note 8*	-	*10*	*15*	*mA*
Sleep Mode Current for V_{DD}	$I_{DD, SLEEP}$		-	1	5	μA
Sleep Mode Current for V_{CC}	$I_{CC, SLEEP}$		-	2	10	μA

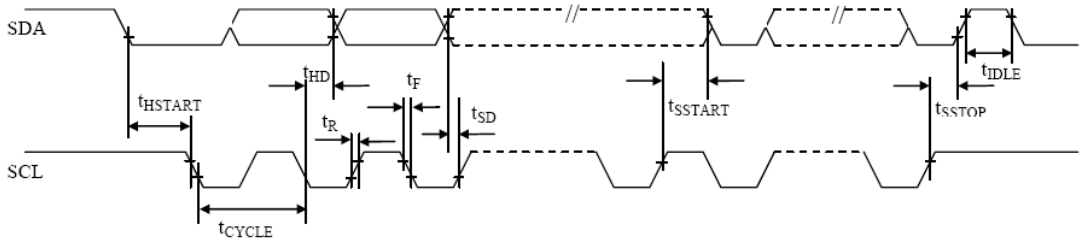
Note 5 & *6*: Brightness (L_{br}) and Supply Voltage for Display (V_{CC}) are subject to the change of the panel characteristics and the customer's request.
Note 7: V_{DD} = 2.8V, V_{CC} = 7.25V, 100% Display Area Turn on.
Note 8: V_{DD} = 2.8V, V_{CC} = 7.25V, 100% Display Area Turn on.
* Software configuration follows Section 4.4 Initialization.

3.3 AC Characteristics

3.3. 1 I^2C Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	2.5	-	μs
t_{HSTART}	Start Condition Hold Time	0.6	-	μs
t_{HD}	Data Hold Time (for "SDA_{OUT}" Pin)	0	-	ns
	Data Hold Time (for "SDA_{IN}" Pin)	300		
t_{SD}	Data Setup Time	100	-	ns
t_{SSTART}	Start Condition Setup Time (Only relevant for a repeated Start condition)	0.6	-	μs
t_{SSTOP}	Stop Condition Setup Time	0.6	-	μs
t_R	Rise Time for Data and Clock Pin		300	ns
t_F	Fall Time for Data and Clock Pin		300	ns
t_{IDLE}	Idle Time before a New Transmission can Start	1.3	-	μs

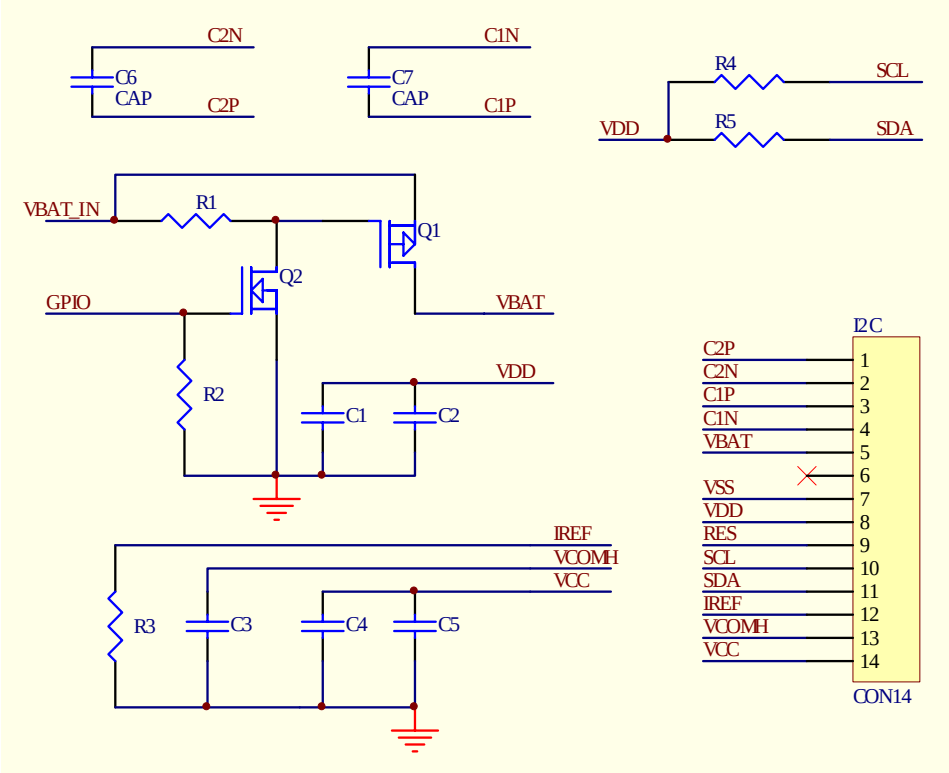
* (V_{DD} - V_{SS} = 1.65V to 3.3V, T_a = 25°C)



3.3.2 I²C Interface with Internal Charge Pump

特别提醒(Special Tips):主板设计务必加电子开关，否则，可能引起漏电流现象

(When design main board, Please add Electronic Switch circuit, otherwise, will be caused leak current)



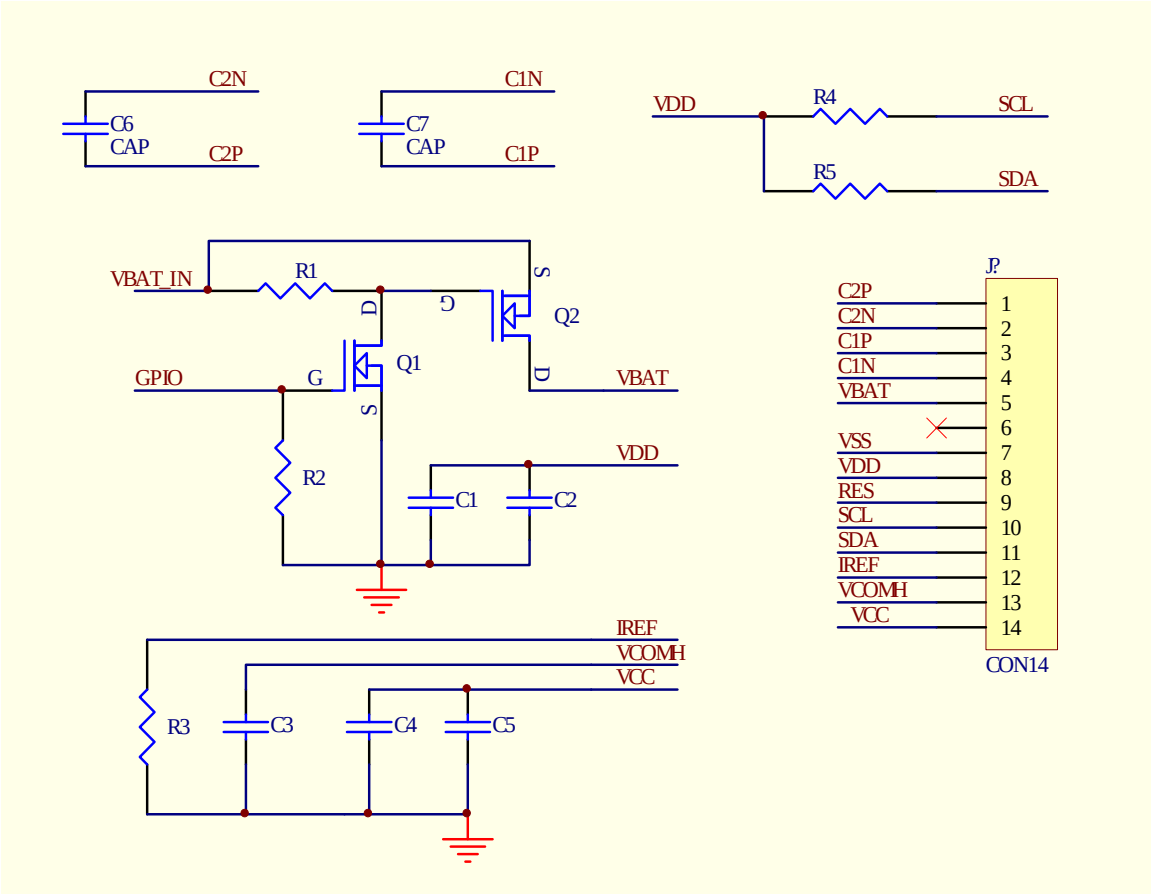
Recommended Components:

C1,:	0.1μF / 6.3V, X5R
C2:	4.7μF / 6.3V, X5R
C3:	2.2μF/ 16V, X7R
C4:	4.7μF / 16V, X7R
C5:	0.1μF / 16V, X7R
C6,C7:	1μF / 16V, X7R
R3:	390KΩ, R3 = (Voltage at IREF - VSS) / IREF
R2, R1:	47kΩ
R4, R5:	4. 7kΩ
Q1:	FDN338P
Q2:	FDN335N

Notes:

VDD:	1.65~3.3V, it should be equal to MPU I/O voltage.
VBAT_in:	3.5~4.2V

3.3.2 I²C Interface with Internal Charge Pump



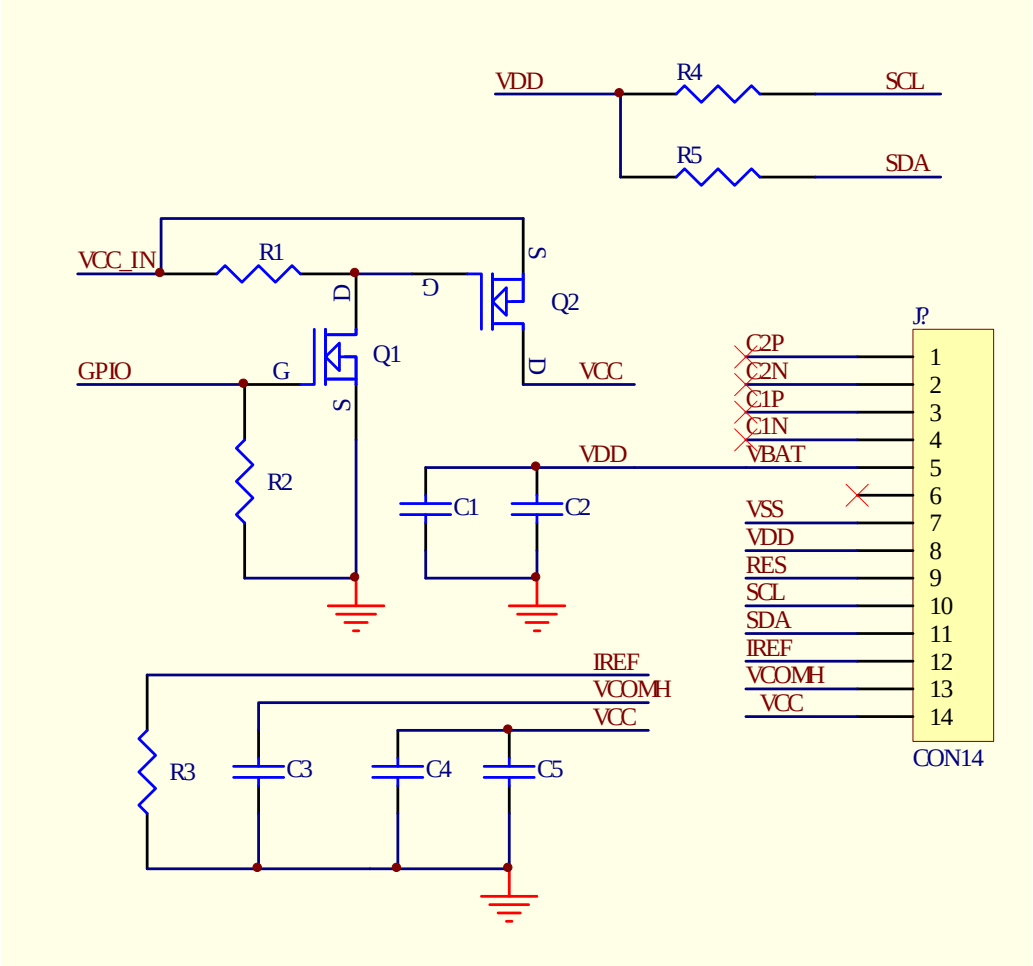
Recommended Components:

C1,:	0.1μF / 6.3V, X5R
C2:	4.7μF / 6.3V, X5R
C3:	2.2μF/ 16V, X7R
C4:	4.7μF / 16V, X7R
C5:	0.1μF / 16V, X7R
C6,C7:	1μF / 16V, X7R
R3:	560KΩ, R3 = (Voltage at IREF - VSS) / IREF
R2, R1:	47kΩ
R4, R5:	4. 7kΩ
Q1:	FDN338P
Q2:	FDN335N

Notes:

VDD:	1.65~3.3V, it should be equal to MPU I/O voltage.
VBAT_in:	3.5~4.2V

3.3.3 I²C Interface with External VCC



Recommended Components:

C1,:	0.1μF / 6.3V, X5R
C2:	4.7μF / 6.3V, X5R
C3:	2.2μF/ 16V, X7R
C4:	4.7μF / 16V, X7R
C5:	0.1μF / 16V, X7R
R3:	560KΩ, R3 = (Voltage at IREF - VSS) / IREF
R2, R1:	47kΩ
R4, R5:	4. 7kΩ
Q1:	FDN338P
Q2:	FDN335N

Notes:

VDD:	1.65~3.3V, it should be equal to MPU I/O voltage.
VCC_in:	7~7.5V