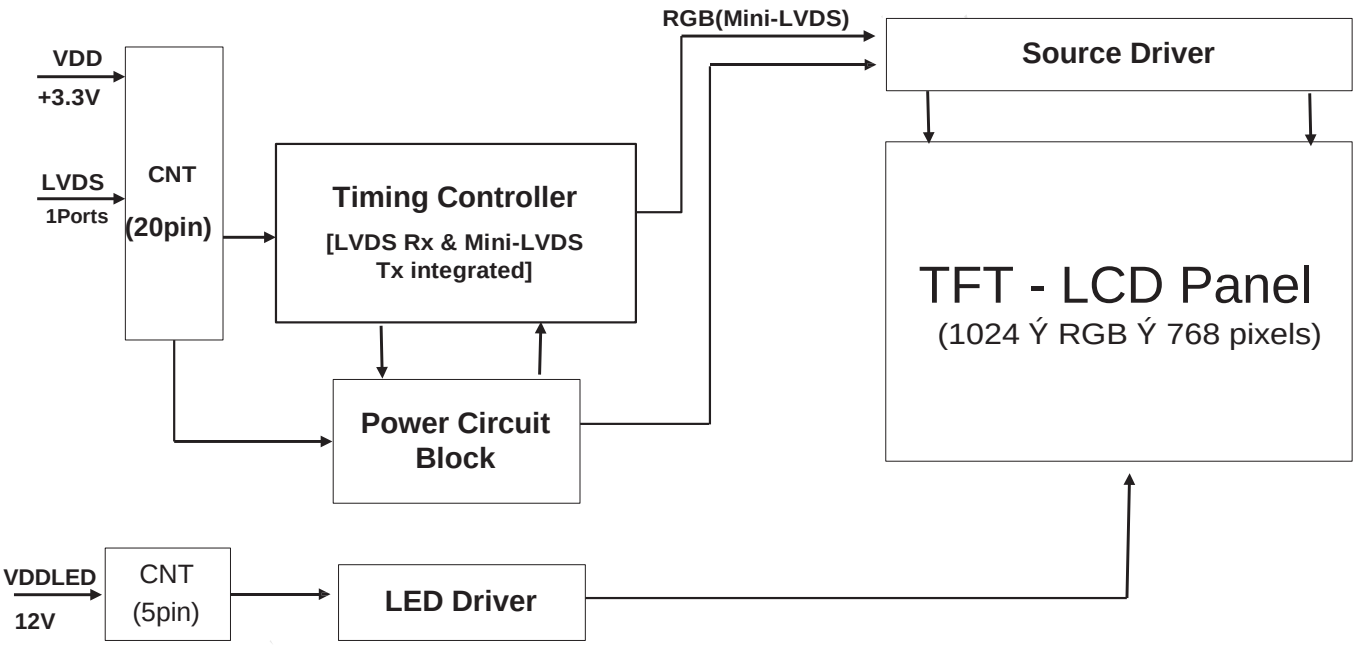
1.0 GENERAL DESCRIPTION

1.1 Introduction

DV150X0M-N10 is a color active matrix TFT LCD MDL using amorphous silicon TFT's (Thin Film Transistors) as an active switching devices. This MDL has a 15 inch diagonally measured active area with XGA resolutions (1024 horizontal by 768 vertical pixel array). Each pixel is divided into RED, GREEN, BLUE dots which are arranged in vertical stripe and this module can display 16.7M colors. The TFT-LCD MDL panel is adapted for a low reflection and higher color type.



1.2 Features

- LVDS interface with 1 pixel / clock
- High-speed response
- Low color shift image quality
- 6-bit +FRC color depth, display 16.7M colors
- Wide viewing angle
- DE (Data Enable) only mode
- ADS technology is applied for high display quality
- RoHS compliant

1.3 Application

- Commercial Digital Display
- Display Terminals for Control System
- Landscape and Portrait Display，7*24 & Indoor lifetime of one year。

1.4 General Specification

< Table 1. General Specifications >

Parameter	Specification	Unit	Remarks
Active area	304.128(H) × 228.096(V)	mm	
Number of pixels	1024(H) ×768(V)	pixels	
Pixel pitch	0.297(H) ×0.297(V)	mm	
Pixel arrangement	Pixels RGB Vertical stripe		
Display colors	16.7M	colors	6bits+FRC
Display mode	Normally Black		
Dimensional outline	326.5(H) × 253.5(V) ×9.7(Total)	mm	Detail refer to drawing
Weight	930	g	
Power Consumption	8.72	Watt	Typ.
Bezel width (L/R/U/D)	10/10/11.7/11.7	mm	
Surface Treatment	Haze 25%, 3H		
Back-light	E-LED Light bar Type		
LED life	50000		
Display Direction	landscape & Portrait		

2.0 ABSOLUTE MAXIMUM RATINGS

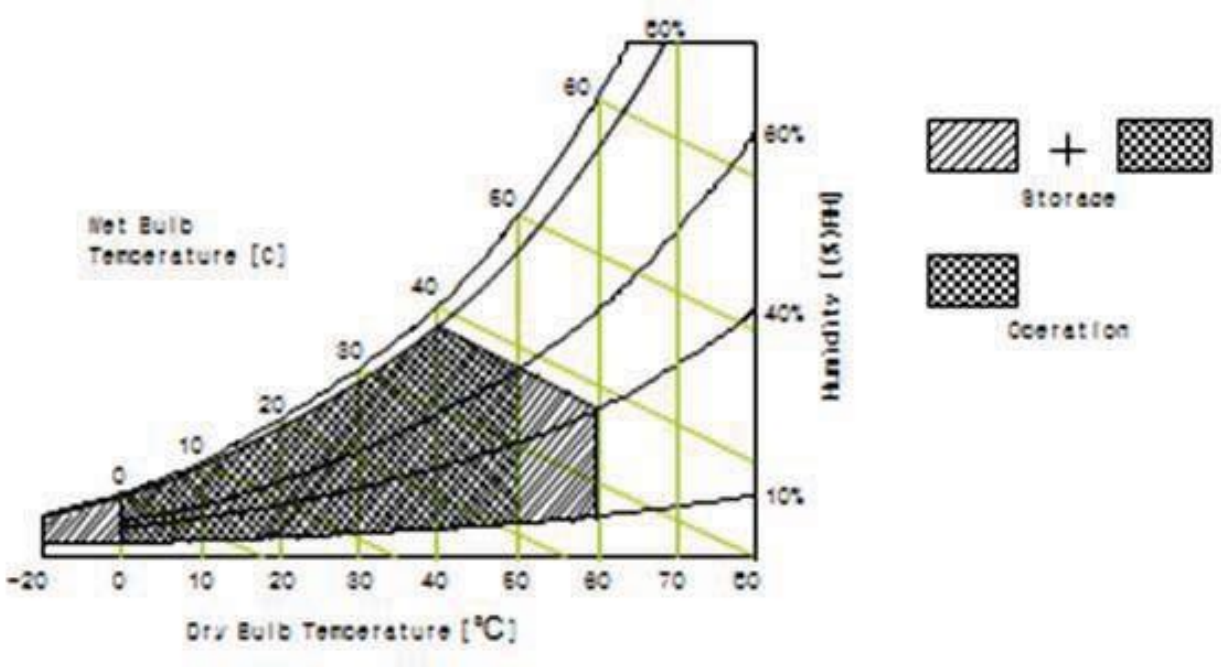
The followings are maximum values which, if exceed, may cause faulty operation or damage to the unit. The operational and non-operational maximum voltage and current values are listed in Table 2.

< Table 2. Open Cell Electrical Specifications >

[VSS=GND=0V]

Parameter	Symbol	Min.	Max.	Unit	Remark
Power Supply Voltage	VDD	-0.3	4	V	Ta = 25 ć
Operating Temperature	T_{OP}	-20	+70	ć	Note 1
Storage Temperature	T_{SUR}	-20	+70	ć	
	T_{ST}	-20	+70	ć	
Operating Ambient Humidity	Hop	10	90	%RH	
Storage Humidity	Hst	10	90	%RH	

Note 1 : Temperature and relative humidity range are shown in the figure below.
Wet bulb temperature should be 39 ć max. and no condensation of water.



3.0 ELECTRICAL SPECIFICATIONS

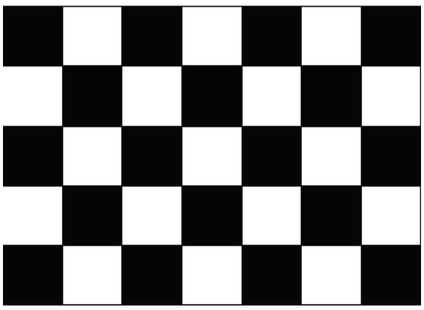
3.1 TFT LCD Open Cell

< Table 3. Open Cell Electrical Specifications >

[Ta =25±2 ℃]

Parameter		Symbol	Values			Unit	Remark
			Min	Typ	Max		
Power Supply Input Voltage		VDD	3.0	3.3	3.6	V	Note 1
Power Supply Current		IDD	-	410	740	mA	
Power Supply Ripple Voltage		VRP	-	-	300	mV	
Rush Current		IRUSH	-	2	3	A	Note 2
LVDS Interface	Differential Input High Threshold Voltage	VLVTH	-	-	+100	mV	VLVC=1.2V
	Differential Input Low Threshold Voltage	VLVTL	-100	-	-	mV	
	Common Input Voltage	VLVC	0.7	-	1.6	V	
CMOS Interface	Input High Threshold Voltage	VIH	0.7VDD	-	VDD	V	
	Input Low Threshold Voltage	VIL	0	-	0.3VDD	V	
Power Consumption		PD		0.8	1.3	W	
		PBL		7.92	8.71		Note 3
		Ptotal		8.72	10.1		

Note 1 : The supply voltage is measured and specified at the interface connector of LCM.
The current draw and power consumption specified is for VDD=3.3V,
Test Pattern of power supply current
a) Typ : Mosaic 7X5 (L0/L255) b) Max : Vline Subline (L255))



Note 2 : The duration of rush current is about 2ms and rising time of Power Input is 1ms(min)
Note 3: Calculated value for reference (Input pins*VPIN ×IPIN) excluding inverter loss.

3.0 ELECTRICAL SPECIFICATIONS

3.2 Backlight Unit

< Table 4. Backlight Unit Electrical Specifications >

[Ta =25℃2 ℃]

Parameter			Min.	Typ.	Max.	Unit	Remarks
LED Driver Power Supply Voltage		H_{VDD}	10.8	12	12.6	V	
LED Driver Power Supply Current		I_{HVDD}	550	600	700	mA	
EN Control Level	Backlight on	V_{ENH}	3	3.3	3.6	V	EN logic high v oltage
	Backlight off	V_{ENL}	0	0	0.6	V	EN logic low vol tage
PWM Control Level	PWM High Level	V_{PML}	3	3.3	3.6	V	
	PWM Low Level	V_{PML}	0	0	0.6	V	
PWM Control Frequency		F_{PWM}	0.12	-	20	KHz	Refer to customer comments
Duty Ratio		-	5	-	100	%	
LED Life-Time		N/A	50,000	-	-	Hour	Note4
LED Light Bar Input Voltage Per Input Pin		VPIN	32.4	36	39.6	V	
LED Light Bar Input Current Per Input Pin		IPIN	-	55	-	mA	Note2
LED Power Consumption		PBL	-	7.92	8.71	W	Note3

LED bar consists of 48LED packages,4 strings(parallel)*12packages(serial)
Note1: There are one light bar ,and the specified current is input LED chip 100% duty current
Note2: The sense current of each input pin is 55mA
Note3: PBL=4 Input pins*VPIN ÝIPIN
Note4: The lifetime is determined as the time at which luminance of LED become 50% of the initial brightness or not normal lighting at IPIN=55mA on condition of continuous operating at 25 ±2 ℃

4.0 INTERFACE CONNECTION

4.1 Open Cell Input Signal & Power

- LVDS Connector : 39(240420. +’ UX)USVGZOHRK.

< Table 4. Open Cell Input Connector Pin Configuration >

Pin No	Symbol	Description	Pin No	Symbol	Description
1	VDD	Power Supply为3.3V(typ.)	11	RIN2-	-LVDS differential data input 2
2	VDD	Power Supply,3.3V(typ.)	12	RIN2+	+LVDS differential data input 2
3	VSS	Ground	13	VSS	Ground
4	NC	No Connection	14	CLKIN-	-LVDS differential clock input CLK
5	RIN0-	-LVDS differential data input 0	15	CLKIN+	+LVDS differential clock input CLK
6	RIN0+	+LVDS differential data input 0	16	VSS	Ground
7	VSS	Ground	17	RIN3-	-LVDS differential data input 3
8	RIN1-	-LVDS differential data input 1	18	RIN3+	+LVDS differential data input 3
9	RIN1+	+LVDS differential data input 1	19	VSS	Ground
10	VSS	Ground	20	NC	No Connection

4.2 LED Light Bar

-LED connector(厂商)/420531.80-4.(型号UX)USVGZ0HRK

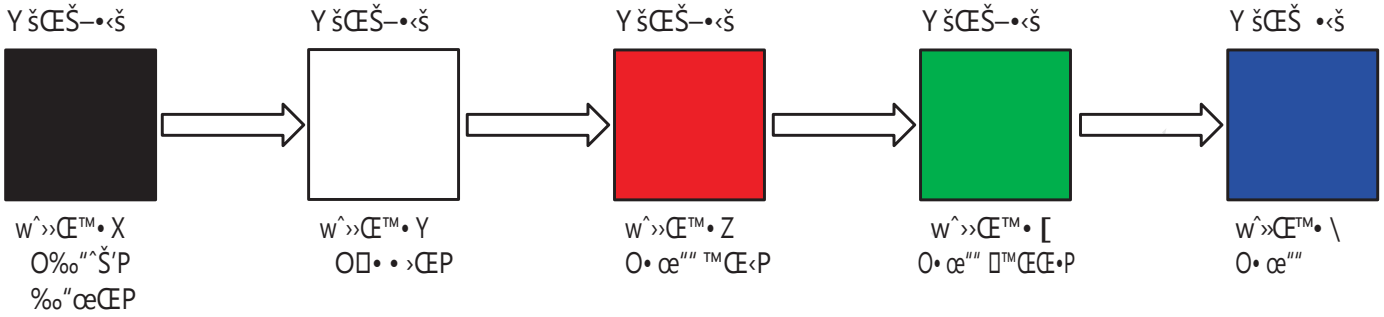
< Table 5. LED Light Bar>

Pin No	Symbol	Description
1	NC	No Connection
2	Dimming	PWM Dimming
3	Enable	3.3V On / 0V-Off
4	GND	Ground
5	VCC	12V

Notes : 1. NC(Not Connected) : This pins are only used for BOE internal operations.

2. Input Level of LVDS signal is based on the EIA-644 Standard.

BIST Pattern



4.2 LVDS Interface

- LVDS Receiver : Timing Controller (LVDS Rx merged) / LVDS Data : Pixel Data

< Table 6. Open Cell Input Connector Pin Configuration >

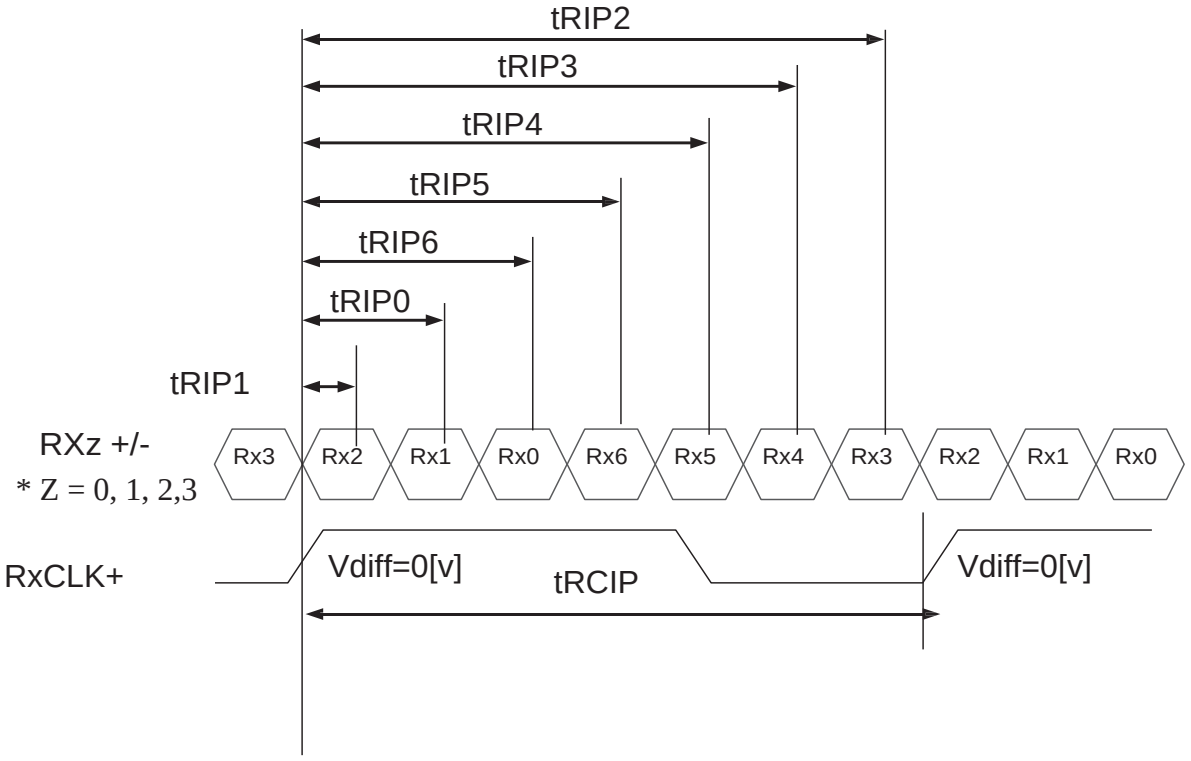
	Input Signal	Transmitter		Interface		HT236F01-100 (CN11)	Remark
		Pin No.	Pin No.	System (Tx)	TFT-LCD (Rx)	Pin No.	
LVDS	OR0	51	48 47	OUT0- OUT0+	RXO0- RXO0+	1 2	
	OR1	52					
	OR2	54					
	OR3	55					
	OR4	56					
	OR5	3					
	OG0	4					
	OG1	6	46 45	OUT1- OUT1+	RXO1- RXO1+	3 4	
	OG2	7					
	OG3	11					
	OG4	12					
	OG5	14					
	OB0	15					
	OB1	19					
	OB2	20	42 41	OUT2- OUT2+	RXO2- RXO2+	5 6	
	OB3	22					
	OB4	23					
	OB5	24					
	Hsync	27					
	Vsync	28					
	DE	30					
	MCLK	31	40 39	CLK OUT- CLK OUT+	RXO CLK- RXO CLK+	8 9	
	OR6	50	38 37	OUT3- OUT3+	RXO3- RXO3+	10 11	
	OR7	2					
	OG6	8					
	OG7	10					
	OB6	16					
	OB7	18					
	RSVD	25					

4.3 LVDS Rx Interface Timing Parameter

The specification of the LVDS Rx interface timing parameter is shown in Table 6.

<Table 7. LVDS Rx Interface Timing Specification>

Item	Symbol	Min	Typ	Max	Unit	Remark
CLKIN Period	tRCIP	10.31	13.47	15.87	nsec	
Input Data 0	tRIP1	0.5 *tRCIP/7-0.4	0.5 *tRCIP/7	0.5 *tRCIP/7 +0.4	nsec	
Input Data 1	tRIP0	1.5 *tRCIP/7 -0.4	1.5 *tRCIP/7	1.5 *tRCIP/7 +0.4	nsec	
Input Data 2	tRIP6	2.5 *tRCIP/7-0.4	2.5 *tRCIP/7	2.5 *tRCIP/7+0.4	nsec	
Input Data 3	tRIP5	3.5 *tRCIP/7-0.4	3.5 *tRCIP/7	3.5 *tRCIP/7+0.4	nsec	
Input Data 4	tRIP4	4.5 *tRCIP/7-0.4	4.5 *tRCIP/7	4.5 *tRCIP/7+0.4	nsec	
Input Data 5	tRIP3	5.5 *tRCIP/7-0.4	5.5 *tRCIP/7	5.5 *tRCIP/7+0.4	nsec	
Input Data 6	tRIP2	6.5 *tRCIP/7-0.4	6.5 *tRCIP/7	6.5 *tRCIP/7+0.4	nsec	



* Vdiff = (RXz+)-(RXz-),…. ,(RXCLK+)-(RXCLK-)