

80C286

CHMOS MICROPROCESSOR WITH MEMORY MANAGEMENT AND PROTECTION

- High Speed CHMOS III Technology
- Pin for Pin, Clock for Clock, and Functionally Compatible with the HMOS 80286

(See 80286 Data Sheet, Order #210253)

- Stop Clock Capability
 - Uses Less Power (see I_{CCS} Specification)

- 12.5 MHz Clock Rate

- Available in a Variety of Packages:
 - 68 Pin PLCC (Plastic Leaded Chip Carrier)
 - 68 Pin PGA (Pin Grid Array)

(See Packaging Spec., Order #231389)

INTRODUCTION

The 80C286 is an advanced 16 bit CHMOS III microprocessor designed for multi-user and multi-tasking applications that require low power and high performance. The 80C286 is fully compatible with its predecessor the HMOS 80286 and object-code compatible with the 8086 and 80386 family of products. In addition, the 80C286 has a power down mode which uses less power, making it ideal for mobile applications. The 80C286 has built-in memory protection that maintains a four level protection mechanism for task isolation, a hardware task switching facility and memory management capabilities that map 2^{30} bytes (one gigabyte) of virtual address space per task (per user) into 2^{24} bytes (16 megabytes) of physical memory.

The 80C286 is upward compatible with 8086 and 8088 software. Using 8086 real address mode, the 80C286 is object code compatible with existing 8086, 8088 software. In protected virtual address mode, the 80C286 is source code compatible with 8086, 8088 software which may require upgrading to use virtual addresses supported by the 80C286's integrated memory management and protection mechanism. Both modes operate at full 80C286 performance and execute a superset of the 8086 and 8088 instructions.

The 80C286 provides special operations to support the efficient implementation and execution of operating systems. For example, one instruction can end execution of one task, save its state, switch to a new task, load its state, and start execution of the new task. The 80C286 also supports virtual memory systems by providing a segment-not-present exception and restartable instructions.

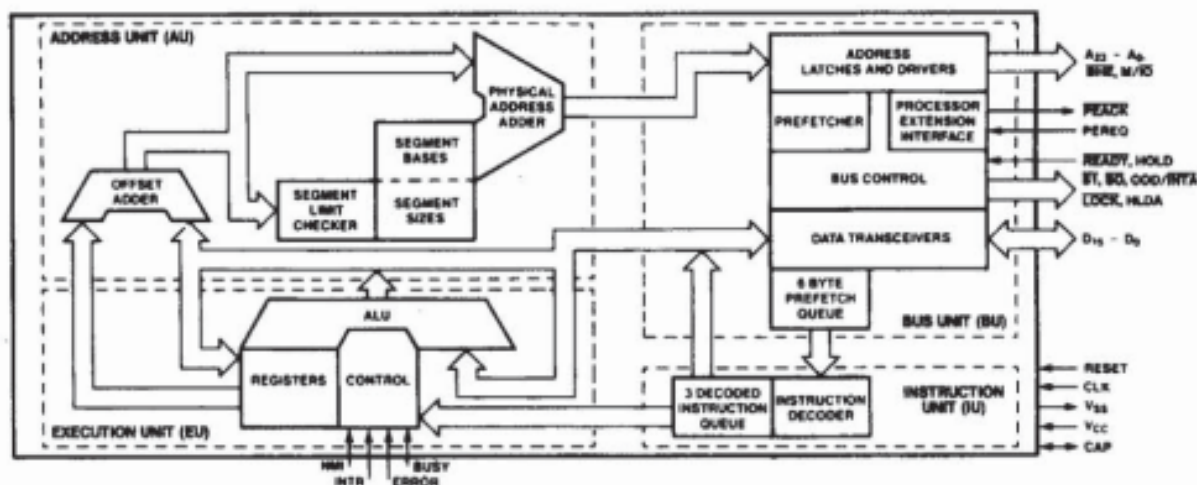


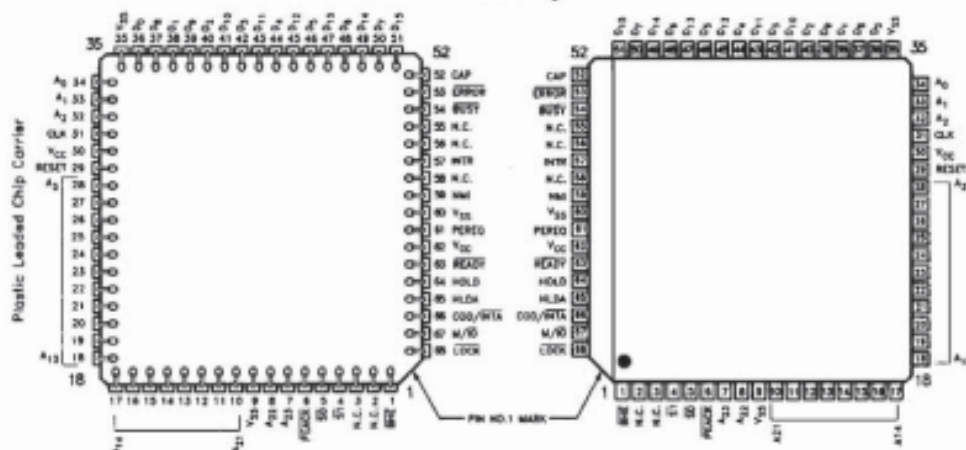
Figure 1. 80C286 Internal Block Diagram

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Component Pad Views—As viewed from underside of component when mounted on the board.

P.C. Board Views—As viewed from the component side of the P.C. board.

Plastic Leaded Chip Carrier

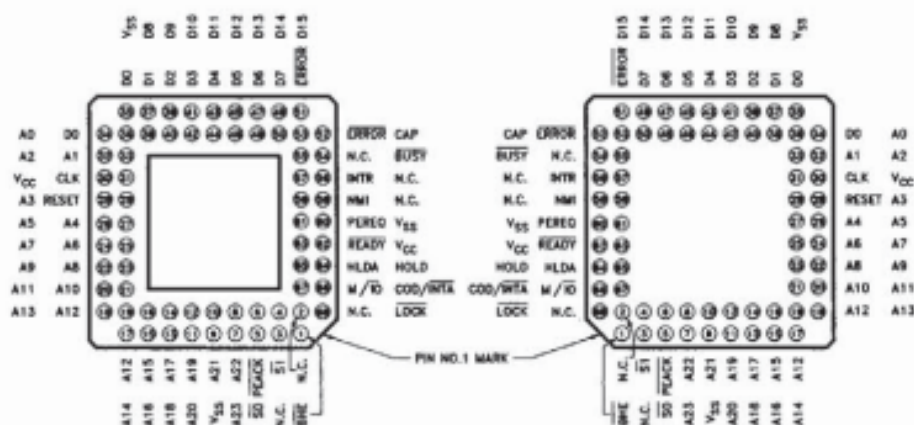


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NOTE:

N.C. signals must not be connected

Pin Grid Array



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Figure 2. 80C286 Pin Configuration

Table 1. Pin Description

The following pin function descriptions are for the 80C286 microprocessor:

Symbol	Type	Name and Function
CLK	I	SYSTEM CLOCK provides the fundamental timing for 80C286 systems. It is divided by two inside the 80C286 to generate the processor clock. The internal divide-by-two circuitry can be synchronized to an external clock generator by a LOW to HIGH transition on the RESET input.
D ₁₅ –D ₀	I/O	DATA BUS inputs data during memory, I/O, and interrupt acknowledge read cycles; outputs data during memory and I/O write cycles. The data bus is active HIGH and floats to 3-state OFF* during bus hold acknowledge.
A ₂₃ –A ₀	O	ADDRESS BUS outputs physical memory and I/O port addresses. A ₀ is LOW when data is to be transferred on pins D ₇ –D ₀ . A ₂₃ –A ₁₆ are LOW during I/O transfers. The address bus is active HIGH and floats to 3-state OFF* during bus hold acknowledge.
BHE	O	BUS HIGH ENABLE indicates transfer of data on the upper byte of the data bus. D ₁₅ –D ₈ . Eight-bit oriented devices assigned to the upper byte of the data bus would normally use BHE to condition chip select functions. BHE is active LOW and floats to 3-state OFF* during bus hold acknowledge.

*See bus hold circuitry section.