Introduction

NVIDIA® MFS1S50 is a QSFP56 VCSEL-based (Vertical Cavity Surface-Emitting Laser), cost-effective 200Gb/s to 2 x 100Gb/s active optical splitter cable (AOC) designed for use in 200Gb/s InfiniBand (IB) HDR (High Data Rate) and 200GbE systems.

The MFS1S50 cable is compliant with SFF-8665 for the QSFP56 pluggable solution. It provides connectivity between system units with a 200Gb/s connector on one side and two separate 100Gb/s connectors on the other side, such as a switch and two servers. The cable connects data signals from each of the 4 MMF (Multi Mode Fiber) pairs on the single QSFP56 end to the dual pair of each of the QSFP56 multiport ends. Each QSFP56 end of the cable comprises an EEPROM providing product and status monitoring information, which can be read by the host system.

NVIDIA's unique-quality cable solutions provide power-efficient connectivity for data center interconnects. It enables higher port bandwidth, density and configurability at a low cost, and reduced power requirement in the data centers.

Rigorous production testing ensures the best out-of-the-box installation experience, performance and durability.

Note

Images are for illustration purposes only. Product labels, colors, and lengths may vary.

Key Features

- Supports IBTA IB HDR and 200GbE
- 200Gb/s HDR to 2x100Gb/s HDR100 data rate
- 200GbE to 2x100GbE data rate
- 4x 50Gb/s PAM4 modulation
- Programmable Rx output amplitude and pre-emphasis
- SFF-8665 compliant QSFP56 port
- Single 3.3V power supply
- 4.5W power consumption (typ., 200G end)
- Up to 30m length
- Hot pluggable
- RoHS compliant
- SFF-8636 compliant I^2C management interface

Pin Description

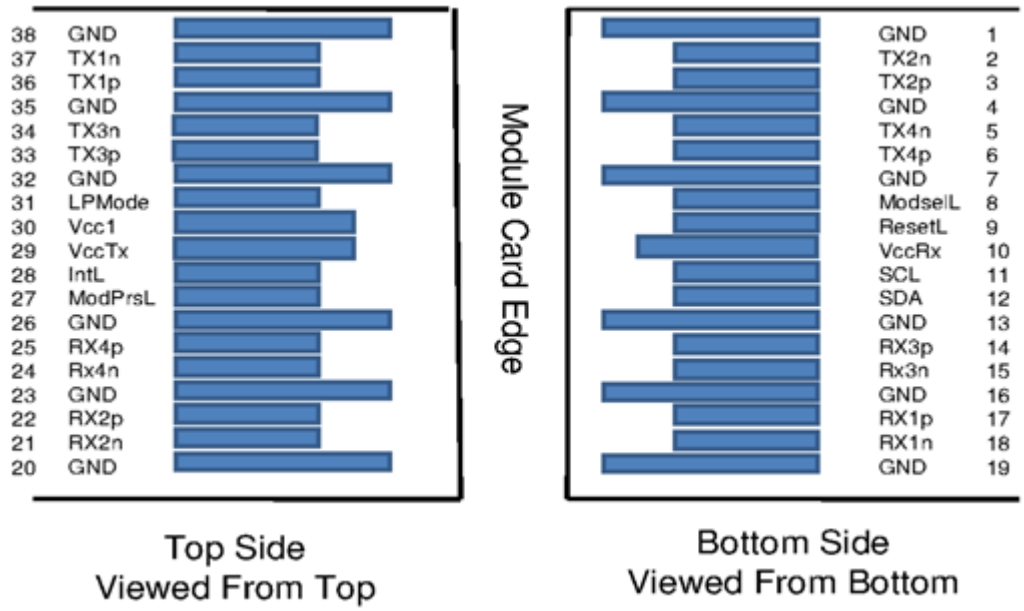
The Active Optical Cable (AOC) pin assignment is SFF-8679 compliant.

QSFP56 Pin Description 200Gb/s End

Pin	Symbol	Description	Pin	Symbol	Description
1	Ground	Ground	20	Ground	Ground
2	Tx2n	Connected to Port 1 lane Rx2 Inverted Data	21	Rx2n	Connected to Port 1 lane Tx2 Inverted Data
3	Tx2p	Connected to Port 1 lane Rx2 Non-Inverted Data	22	Rx2p	Connected to Port 1 lane Tx2 Non-Inverted Data
4	Ground	Ground	23	Ground	Grounds
5	Tx4n	Connected to Port 2 lane Rx2 Non-Inverted Data	24	Rx4n	Connected to Port 2 lane Tx2 Inverted Data
6	Tx4p	Connected to Port 2 lane Rx2 Inverted Data	25	Rx4p	Connected to Port 2 lane Tx2 Non-Inverted Data
7	Ground	Ground	26	Ground	Ground
8	Mod-SelL	Cable Select	27	ModPrsL	Cable Present
9	ResetL	Cable Reset	28	IntL	Interrupt
10	Vcc Rx	+3.3V Power supply receiver	29	Vcc Tx	+3.3V Power supply transmitter
11	SCL	2-wire serial interface clock	30	Vcc1	+3.3V Power Supply
12	SDA	2-wire serial interface data	31	LPMode	Low Power Mode

Pin	Symbol	Description	Pin	Symbol	Description
13	Ground	Ground	32	Ground	Ground
14	Rx3p	Connected to Port 2 lane Tx1 Non-Inverted Data	33	Tx3p	Connected to Port 2 lane Rx1 Non-Inverted Data
15	Rx3n	Connected to Port 2 lane Tx1 Inverted Data	34	Tx3n	Connected to Port 2 lane Rx1 Inverted Data
16	Ground	Ground	35	Ground	Ground
17	Rx1p	Connected to Port 1 lane Tx1 Non-Inverted Data	36	Tx1p	Connected to Port 1 lane Rx1 Non-Inverted Data
18	Rx1n	Connected to Port 1 lane Tx1 Inverted Data	37	Tx1n	Connected to Port 1 lane Rx1 Inverted Data
19	Ground	Ground	38	Ground	Ground

QSFP56 Module Pad Layout



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3	Tx2p	Connected to lane Rx2 Non-Inverted Data	22	Rx2p	Connected to lane Tx2 Non-Inverted Data
4	Ground	Ground	23	Ground	Grounds
5	Not connected	Not connected	24	Not connected	Not connected
6	Not connected	Not connected	25	Not connected	Not connected
7	Ground	Ground	26	Ground	Ground
8	Mod-SelL	Cable Select	27	ModPrsL	Cable Present
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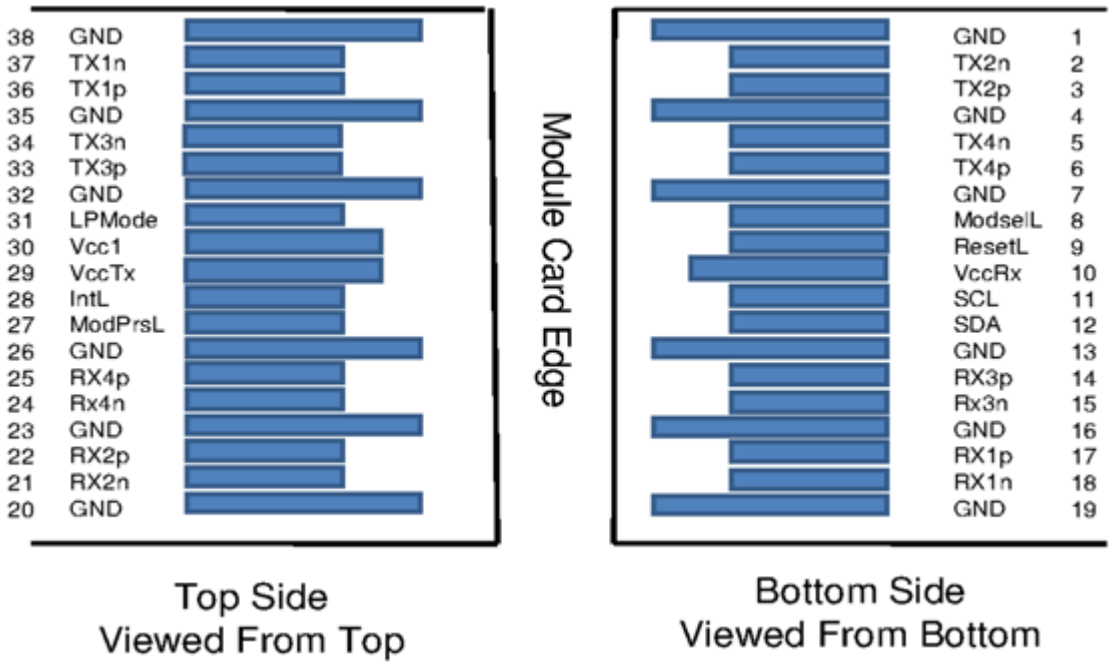
18	Rx1n	Connected to lane Tx1 Inverted Data	37	Tx1n	Connected to lane Rx1 Inverted Data
19	Ground	Ground	38	Ground	Ground

QSFP56 Module Pad Layout

The pinout of the 100Gb/s ends of the cable is identical to the 200Gb/s end except that RF lanes 3 and 4 (pins 5, 6, 14, 15, 24, 25, 33, 34) are not used.



Control Signals

This transceiver is SFF-8636 compliant. This means that the control signals shown in the pad layout support the following functions:

Name	Function	Description
ModPrsL	Output, asserted low	Module Present pin, grounded inside the module. Terminated with pull-up in the host system. Asserted low when the transceiver is inserted, whereby the host detects the presence of the transceiver.
ModSelL	Input, asse	Module Select input pin, terminated high in the module. Only when held low by the host, the module responds to 2-wire serial communication commands. The ModSelL enables multiple modules to share a single 2-wire interface bus.

Name	Function	Description
	rted Low	
ResetL	Input, asserted Low	Reset input pin, pulled high in the module. A low level on the ResetL pin for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state. During reset the host shall disregard all status bits until the module indicates completion of the reset interrupt by asserting IntL signal low with the Data_Not_Ready bit negated. Note that on power up (including hot insertion) the module completes the reset interrupt without requiring a reset.
LPMode	Input, asserted high	Low Power Mode input, pulled up inside the module. The transceiver starts up in low-power mode, i.e. <1.5 W with the two-wire interface active. The host system can read the power class declaration from the transceiver and determine if it has enough power to enable the high-speed operation/high power mode of the transceiver. This can be done by asserting LPMode low or by use of the Power_over-ride and Power_set control bits (Address A0h, byte 93 bits 0,1).
IntL	Output, asserted low	Interrupt Low is an open-collector output, terminated high in the host system. A “Low” indicates a possible module operational fault or a status critical to the host system, e.g. temperature alarm. The host identifies the source of the interrupt using the 2-wire serial interface. The INTL pin is de-asserted “High” after completion of reset, when byte 2 bit 0 (Data Not Ready) is read with a value of ‘0’.

The low-speed signals are Low Voltage TTL (LVTTL) compliant (except for SCL and SDA signals).

Diagnostics and Other Features

The transceiver complies with the SFF-8665 specification and has the following key features:

Physical layer link optimization:

- Programmable Tx input equalization
- Programmable Rx output amplitude
- Programmable Rx output pre-emphasis

- Tx/Rx CDR control

  by default enabled for 100 GbE operation, disable it for 40G operation

Digital Diagnostic Monitoring (DDM):

- Rx receive optical power monitor for each lane
- Tx transmit optical power monitor for each lane
- Tx bias current monitor for each lane
- Supply voltage monitor
- Transceiver case temperature monitor
- Warning and Alarm thresholds for each DDM function (not user changeable)

Other SFF-8636 functions and interrupt indications:

- Tx & Rx LOS indication
- Tx & Rx LOL indication
- Tx fault indication

LOS, LOL, and Tx Fault status flags can be read via the two-wire management interface and are jointly transmitted via the IntL output pin. Relevant advertisement, threshold, and readout registers are found in the SFF-8636 MSA.