

SPECIFICATION

PART NO. : OHEM12864-18

**OLED
Display**
128X64

2.42"

This specification maybe changed without any notice in order to improve performance or quality etc.

Please contact Haresan OLED R&D department for update specification and product status before design for this product or release the order.

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 HARESAN 华尔升		Customer	
Written by	Zhang Yuxuan	Approved by	
Checked by	YangXue yu		
Approved by	ZhangWeicang		

REVISION HISTORY

Rev.	Contents	Date
0.1	Preliminary	2017-7-12
1.0	First release	2017-8-2

■ PHYSICAL DATA

No.	Items:	Specification:	Unit
1	Diagonal Size	2.42	Inch
2	Resolution	128(H) x 64(V)	Dots
3	Active Area	55.01(W) x 27.49(H)	mm ²
4	Outline Dimension (Panel)	60.5(W) x 37.00(H)	mm ²
5	Pixel Pitch	0.43(W) x 0.43(H)	mm ²
6	Pixel Size	0.40(W) x 0.40(H)	mm ²
7	Driver IC	SSD1309ZC	-
8	Display Color	White	-
9	Grayscale	1	Bit
10	Interface	Parallel / Serial/IIC	-
11	IC package type	COG	-
12	Thickness	2.0±0.2	mm
13	Weight	TBD	g
14	Duty	1/64	-

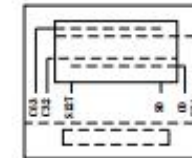
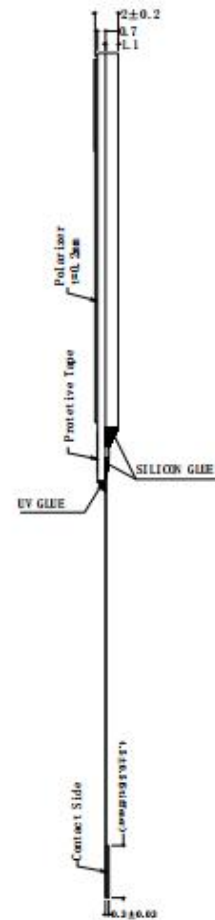
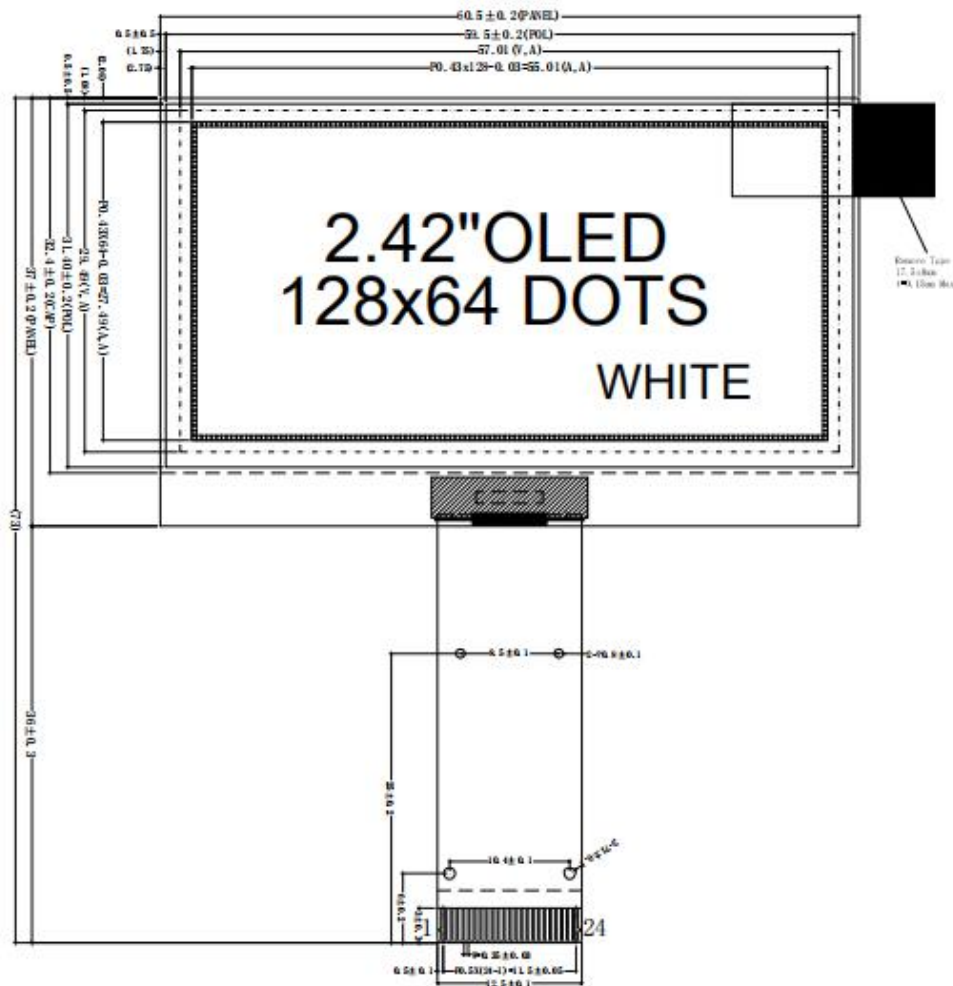
■ ABSOLUTE MAXIMUM RATINGSUnless otherwise specified,(Voltage Referenced to V_{SS})

(Ta = 25℃)

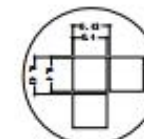
Items		Symbol	Min	Typ.	Max	Unit
Supply Voltage	Logic	V _{DD}	-0.3	-	4.0	V
	Driving	V _{cc}	0	-	17	V
Operating Temperature		Top	-40	-	70	℃
Storage Temperature		Tst	-40	-	85	℃
Humidity		-	-	-	90	%RH

NOTE:

Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect reliability.



COMASEG LAYOUT



Data Detail
SCALE 10X

Customer No.:

HAZARDOUS SUBSTANCES MANAGEMENT STANDARD

☒	ROHS COMPLIANT
☒	ROHS COMPLIANT AND HALOGEN-FREE
☐	RESTRICTED SUBSTANCE CONTROL STANDARD. (VERSION:)

PIN DESCRIPTION

NO.	SYMBOL
1	N. C. (GND)
2	VLSS
3	VSS
4	N. C.
5	VDD
6	BS1
7	BS2
8	CS#
9	RES#
10	D/C#
11	R/W#
12	E/RD#
13	D0
14	D1
15	D2
16	D3
17	D4
18	D5
19	D6
20	D7
21	IREF
22	VCOMH
23	VCC
24	N. C. (GND)

NOTES:

1. OPERATING TEMP:-40° C TO 70° C
2. STORAGE TEMP:-40° C TO 85° C
3. VIEWING DIRECTION:ALL
4. OLED DRIVE IC:SSD1309ZC
5. DISPLAY COLOR: WHITE
6. UNSPECIFIED TOLERANCES: ±0.2mm.
7. () MEANS: DIMENSION FOR REFERENCE
8. THE PROTECTIVE FILM ON THE FRONT SIDE OF OLED MUST BE REMOVED BEFORE ASSEMBLY BY CUSTOMER

■ ELECTRICAL CHARACTERISTICS**◆ DC Characteristics**

Condition(Unless otherwise specified):

Voltage referenced to V_{SS} $V_{DD1}=1.65V$ to $3.5V$ $T_a = 25^{\circ}C$

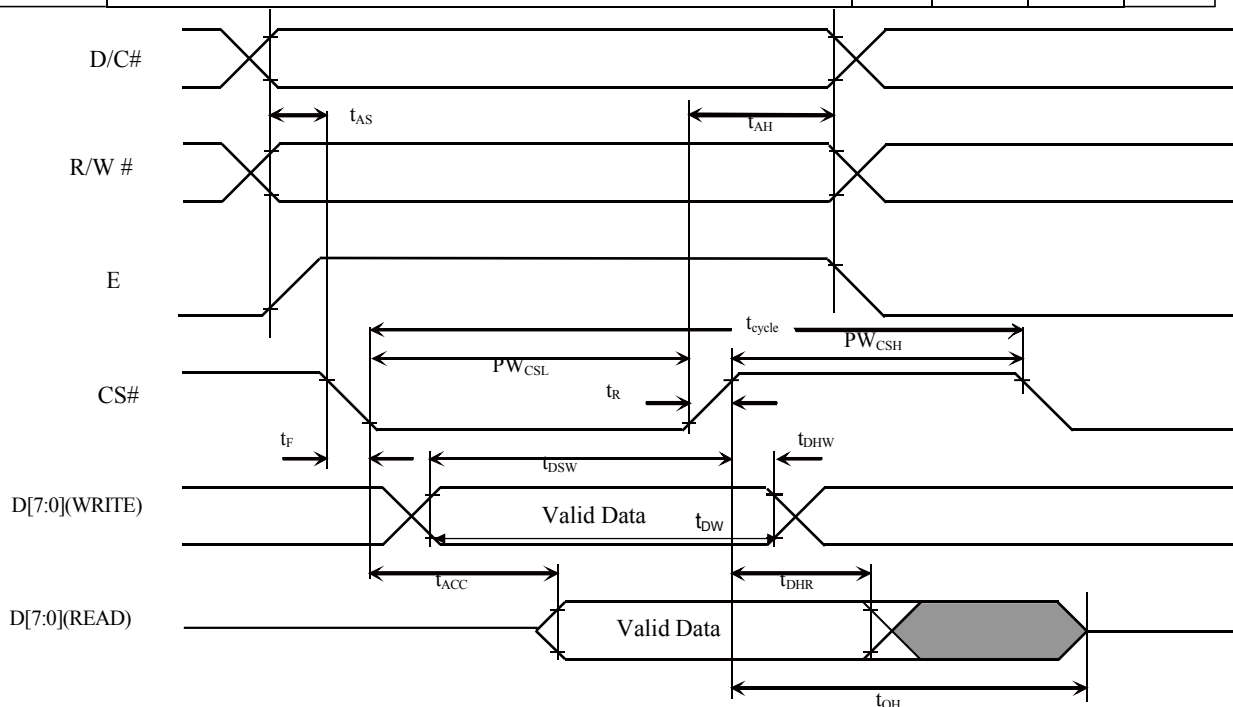
Items		Symbol	Min	Typ.	Max	Unit
Supply Voltage	Logic	V_{DD}	1.65	-	3.5	V
	Operating	V_{cc}	7.0	-	16.0	V
Input Voltage	High Voltage	V_{IH}	$0.8 \times V_{DD}$	-	V_{DD1}	V
	Low Voltage	V_{IL}	V_{SS}	-	$0.2 \times V_{DD}$	V
Output Voltage	High Voltage	V_{OH}	$0.8 \times V_{DD}$	-	V_{DD}	V
	Low Voltage	V_{OL}	V_{SS}	-	$0.2 \times V_{DD}$	V

◆ AC Characteristics

Use 8080/6800-Series MPU Parallel Interface or Serial Interface

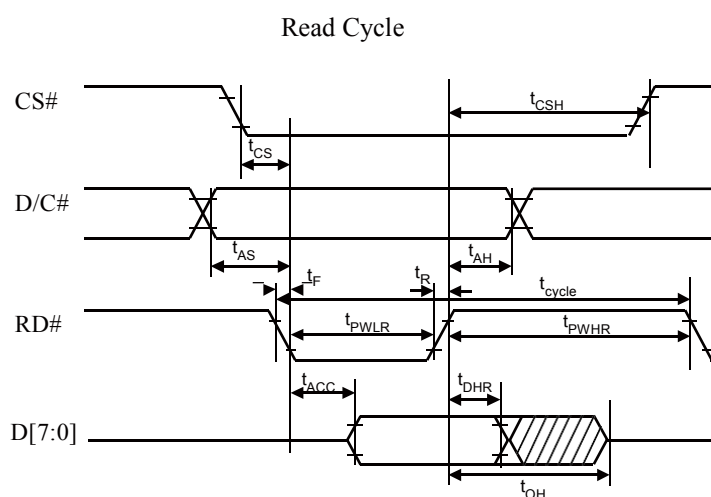
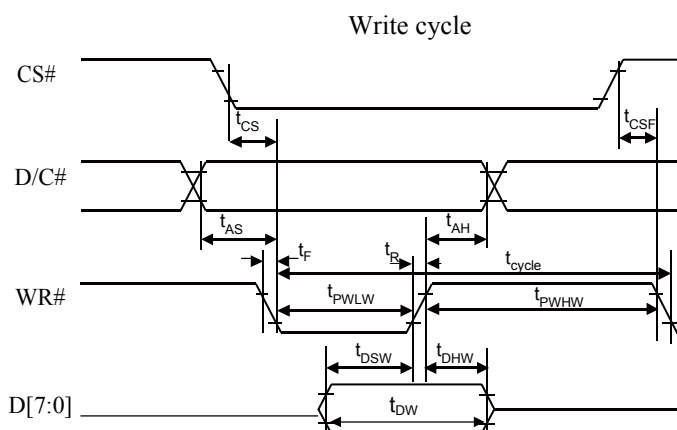
1. 6800 Series MPU Parallel Interface

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	20	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DW}	Data Write Time	80	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	20	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
t_R	Rise Time	-	-	40	ns
t_F	Fall Time	-	-	40	ns



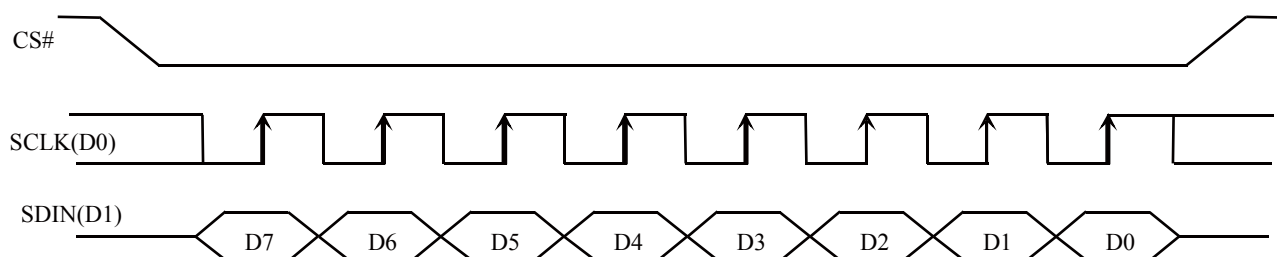
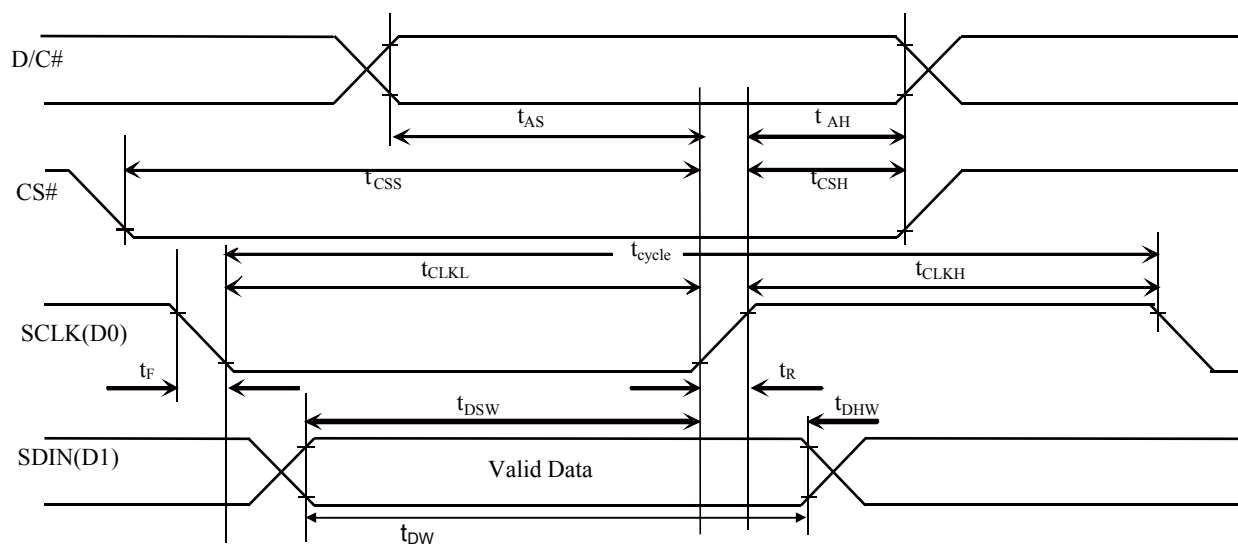
2. 8080 Series MPU Parallel Interface

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	20	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DW}	Data Write Time	70	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
t_{PWLW}	Read Low Time	120	-	-	ns
t_{PWLW}	Write Low Time	60	-	-	ns
t_{PWHR}	Read High Time	60	-	-	ns
t_{PWHW}	Write High Time	60	-	-	ns
t_R	Rise Time	-	-	40	ns
t_F	Fall Time	-	-	40	ns
t_{CS}	Chip select setup time	0	-	-	ns
t_{CSH}	Chip select hold time to read signal	0	-	-	ns
t_{CSF}	Chip select hold time	20	-	-	ns



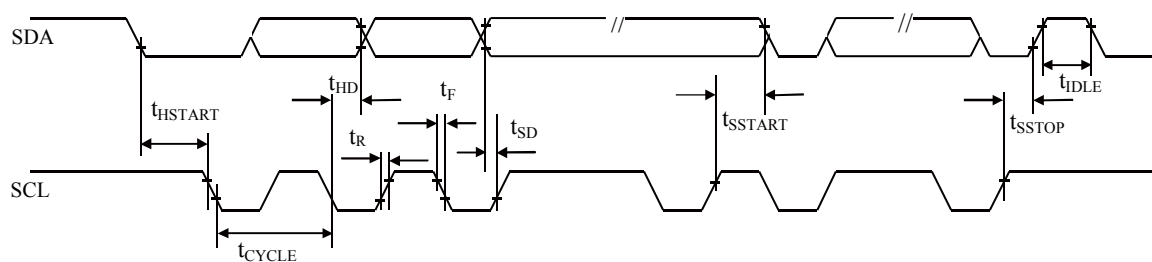
3. Serial Interface

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	-	ns
t_{AS}	Address Setup Time	15	-	-	ns
t_{AH}	Address Hold Time	15	-	-	ns
t_{CSS}	Chip Select Setup Time	20	-	-	ns
t_{CSH}	Chip Select Hold Time	50	-	-	ns
t_{DW}	Data Write Time	55	-	-	ns
t_{DSW}	Write Data Setup Time	15	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{CLKL}	Clock Low Time	50	-	-	ns
t_{CLKH}	Clock High Time	50	-	-	ns
t_R	Rise Time	-	-	40	ns
t_F	Fall Time	-	-	40	ns



4. IIC Interface

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	2.5	-	-	us
t_{HSTART}	Start condition Hold Time	0.6	-	-	us
t_{HD}	Data Hold Time (for “SDA _{OUT} ” pin)	0	-	-	ns
	Data Hold Time (for “SDA _{IN} ” pin)	300	-	-	ns
t_{SD}	Data Setup Time	100	-	-	ns
t_{SSTART}	Start condition Setup Time (Only relevant for a repeated Start condition)	0.6	-	-	us
t_{SSTOP}	Stop condition Setup Time	0.6	-	-	us
t_{R}	Rise Time for data and clock pin	-	-	300	ns
t_{F}	Fall Time for data and clock pin	-	-	300	ns
t_{IDLE}	Idle Time before a new transmission can start	1.3	-	-	us



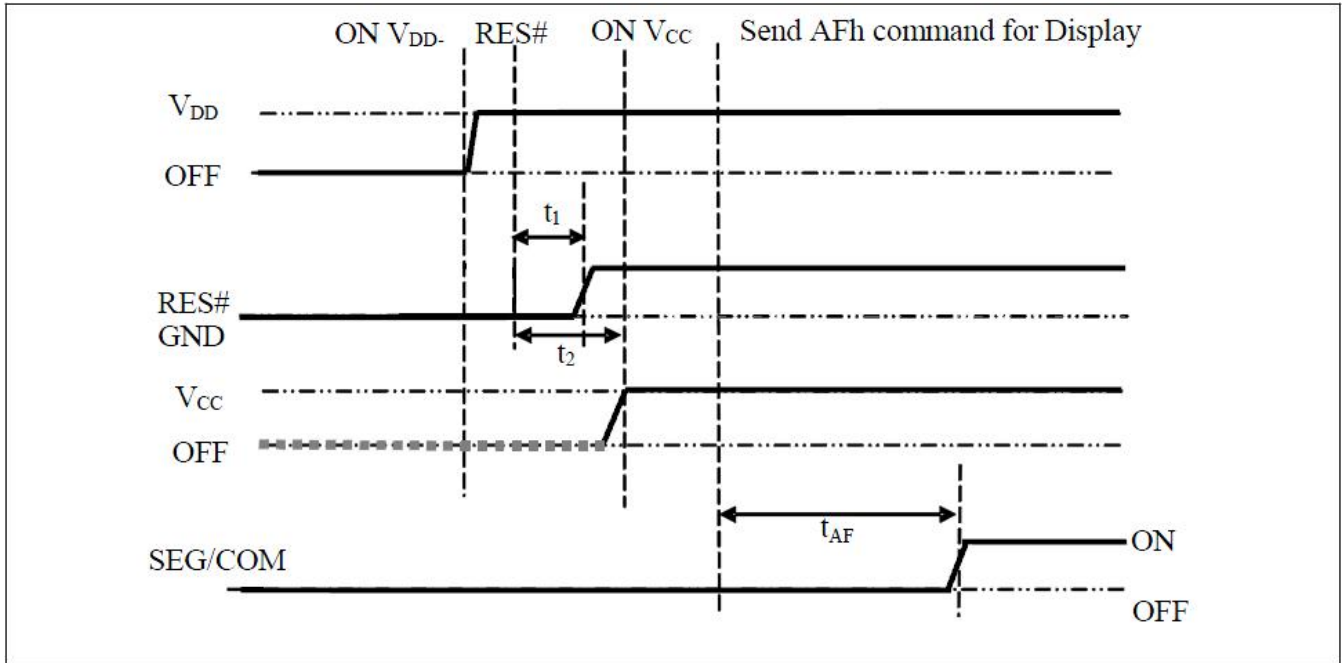
■ TIMING OF POWER SUPPLY

The following figures illustrate the recommended power ON and power OFF sequence of SSD1309

Power ON sequence:

1. Power ON V_{DD}
2. After V_{DD} become stable, set RES# pin LOW (logic low) for at least 3 μ s (t_1) (3) and then HIGH (logic high).
3. After set RES# pin LOW (logic low), wait for at least 3 μ s (t_2). Then Power ON $V_{CC(1)}$
4. After V_{CC} become stable, send command AFh for display ON. SEG/COM will be ON after 100ms (t_{AF}).

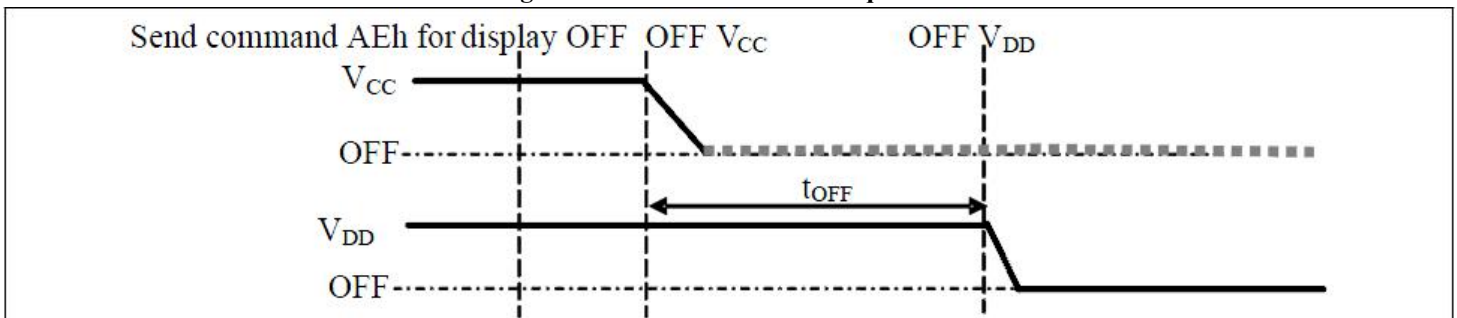
Figure 8-16 : The Power ON sequence



Power OFF sequence:

1. Send command AEh for display OFF.
2. Power OFF $V_{CC(1), (2)}$
3. Power OFF V_{DD} after t_{OFF} . (4) (where Minimum $t_{OFF}=0$ ms, typical $t_{OFF}=100$ ms)

Figure 8-17 : The Power OFF sequence



Note:

- (1) V_{CC} should be kept float (i.e. disable) when it is OFF.
- (2) Power Pins (V_{DD} , V_{CC}) can never be pulled to ground under any circumstance.
- (3) The register values are reset after t_1 .
- (4) V_{DD} should not be Power OFF before V_{CC} Power OFF.

■ ELECTRO-OPTICAL CHARACTERISTICS (Ta=25°C)

Items		Symbol	Min.	Typ.	Max.	Unit	Remark
Operating Luminance		L	50	70	-	cd /m ²	White
Power Consumption		P	-	220	260	mW	30%pixel on
Frame Frequency		Fr	-	100	-	Hz	-
Color Coordinate	White	CIE x	0.26	0.30	0.34	CIE1931	Darkroom
		CIE y	0.29	0.33	0.37		
Response Time	Rise	Tr	-	-	0.02	ms	-
	Decay	Td	-	-	0.02	ms	-
Contrast Ratio*		Cr	10000:1	-	-	-	Darkroom
Viewing Angle		$\triangle \theta$	160	-	-	Degree	-
Operating Life Time*		Top	30000	-	-	Hours	70 cd /m ²

Note:

1. **Test condition** is VDD=3.0V, VCC=14.0V, Contrast= 0xDF.

2. **Contrast ratio** is defined as follows:

$$\text{Contrast ratio} = \frac{\text{Photo - detector output with OLED being "white"}}{\text{Photo - detector output with OLED being "black"}}$$

3. Life Time is defined when the Luminance has decayed to less than 50% of the initial Luminance specification. (Odd and even chess board alternately displayed)
(The initial value should be closed to the typical value after adjusting.)

■ INTERFACE PIN CONNECTIONS

No.	Symbol	Description
1	NC	No connection
2	VSS	Ground.
3	VSS	Ground.
4	NC	No connection
5	VDD	Power supply input: 1.65 - 3.5V
6	BS1	MCU bus interface selection pins.
7	BS2	
8	CS#	This is the chip select input.(active LOW)
9	RES#	This is a reset signal input pad. When RES is set to “L”, the settings are initialized. The reset operation is performed by the RES signal level.
10	D/C	This is the Data/Command control pad that determines whether the data bits are data or a command. A0 = “H”: the inputs at D0 to D7 are treated as display data. A0 = “L”: the inputs at D0 to D7 are transferred to the command registers. In I2C interface, this pad serves as SA0 to distinguish the different address of OLED driver.
11	WR#	This is a MPU interface input pad. When connected to an 8080 MPU, this is active LOW. This pad connects to the 8080 MPU WR signal. The signals on the data bus are latched at the rising edge of the WR signal. When connected to a 6800 Series MPU: This is the read/write control signal input terminal. When W R/ = “H”: Read. When W R/ = “L”: Write.
12	RD#	This is a MPU interface input pad. When connected to an 8080 series MPU, it is active LOW. This pad is connected to the RD signal of the 8080 series MPU, and the data bus is in an output status when this signal is “L”. When connected to a 6800 series MPU , this is active HIGH. This is used as an enable clock input of the 6800 series MPU. When RD = “H”: Enable. When RD = “L”: Disable.
13 - 20	D0-D7	This is an 8-bit bi-directional data bus that connects to an 8-bit or 16-bit standard MPU data bus. When the serial interface is selected, then D0 serves as the serial clock input pad (SCL) and D1 serves as the serial data input pad (SI). At this time, D2 to D7 are set to high impedance. When the I2C interface is selected, then D0 serves as the serial clock input pad (SCL) and D1 serves as the serial data input pad (SDAI). At this time, D2 to D7 are set to high impedance.
21	IREF	This is a segment current reference pad. A resistor should be connected between this pad and VSS. Set the current at 10μA.
22	VCOMH	This is a pad for the voltage output high level for common signals. A capacitor should be connected between this pad and VSS.

23	VCC	Power supply for panel driving voltage. This is also the most positive power voltage supply pin. When charge pump is enabled, a capacitor should be connected between this pin and VSS.
24	NC	No connection

MCU Bus Interface Pin Selection

Pin Name	6800- parallel interface	8080- parallel Interface	4-SPI Interface	IIC Interface
BS1	0	1	0	1
BS2	1	1	0	0

Note:

- (1) 0 is connected to VSS
- (2) 1 is connected to VDD

■ COMMAND TABLE

(D/C#=0, R/W#(WR#)=0, E(RD#)=1) unless specific setting is stated)

1. Fundamental Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0 0	81 A[7:0]	1 A ₇	0 A ₆	0 A ₅	0 A ₄	0 A ₃	0 A ₂	0 A ₁	1 A ₀	Set Contrast Control	Double byte command to select 1 out of 256 contrast steps. Contrast increases as the value increases. (RESET = 7Fh)
0	A4/A5	1	0	1	0	0	1	0	X ₀	Entire Display ON	A4h, X ₀ =0b: Resume to RAM content display (RESET) Output follows RAM content A5h, X ₀ =1b: Entire display ON Output ignores RAM content
0	A6/A7	1	0	1	0	0	1	1	X ₀	Set Normal/Inverse Display	A6h, X[0]=0b: Normal display (RESET) 0 in RAM: OFF in display panel 1 in RAM: ON in display panel A7h, X[0]=1b: Inverse display 0 in RAM: ON in display panel 1 in RAM: OFF in display panel
0	AE/AF	1	0	1	0	1	1	1	X ₀	Set Display ON/OFF	AEh, X[0]=0b: Display OFF (sleep mode) (RESET) AFh X[0]=1b: Display ON in normal mode
0	E3	1	1	1	0	0	0	1	1	NOP	Command for no operation
0 0	FD A[2]	1 0	1 0	1 0	1 1	1 0	1 A ₂	0 1	1 0	Set Command Lock	A[2]: MCU protection status. A[2] = 0b, Unlock OLED driver IC MCU interface from entering command (RESET) A[2] = 1b, Lock OLED driver IC MCU interface from entering command Note (1) The locked OLED driver IC MCU interface prohibits all commands and memory access except the FDh command

2. Scrolling Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description									
0	2C/2D	0	0	1	0	1	1	0	X	Content Scroll Setup	2Ch, X[0]=0, Right Horizontal Scroll by one column									
0	A[7:0]	0	0	0	0	0	0	0	0		2Dh, X[0]=1, Left Horizontal Scroll by one column									
0	B[2:0]	*	*	*	*	*	B ₂	B ₁	0											
0	C[7:0]	0	0	0	0	0	0	0	B ₀											
0	D[2:0]	*	*	*	*	*	D	D	1											
0	E[7:0]	0	0	0	0	0	2	1	D											
0	F[7:0]	F ₇	F ₆	F ₅	F ₄	F ₃	0	0	0											
0	G[7:0]	G	G ₆	G ₅	G ₄	G ₃	F ₂	F ₁	0											
		7					G	G	F ₀		B[2:0] : Define start page address									
							2	1	G		<table><tr><td>000b – PAGE0</td><td>011b – PAGE3</td><td>110b – PAGE6</td></tr><tr><td>001b – PAGE1</td><td>100b – PAGE4</td><td>111b – PAGE7</td></tr><tr><td>010b – PAGE2</td><td>101b – PAGE5</td><td></td></tr></table>	000b – PAGE0	011b – PAGE3	110b – PAGE6	001b – PAGE1	100b – PAGE4	111b – PAGE7	010b – PAGE2	101b – PAGE5	
000b – PAGE0	011b – PAGE3	110b – PAGE6																		
001b – PAGE1	100b – PAGE4	111b – PAGE7																		
010b – PAGE2	101b – PAGE5																			
									0		C[7:0] : Dummy byte (Set as 01h)									
											D[2:0] : Define end page address									
											<table><tr><td>000b – PAGE0</td><td>011b – PAGE3</td><td>110b – PAGE6</td></tr><tr><td>001b – PAGE1</td><td>100b – PAGE4</td><td>111b – PAGE7</td></tr><tr><td>010b – PAGE2</td><td>101b – PAGE5</td><td></td></tr></table>	000b – PAGE0	011b – PAGE3	110b – PAGE6	001b – PAGE1	100b – PAGE4	111b – PAGE7	010b – PAGE2	101b – PAGE5	
000b – PAGE0	011b – PAGE3	110b – PAGE6																		
001b – PAGE1	100b – PAGE4	111b – PAGE7																		
010b – PAGE2	101b – PAGE5																			
											E[7:0] : Dummy byte (Set as 00h)									
											F[7:0] : Define the start column (RESET = 00h)									
											G[7:0] : Define the end column address (RESET = 7Fh)									
											Note									
											⁽¹⁾ The value of D[2:0] must be larger than or equal to B[2:0]									
											⁽²⁾ The value of G[7:0] must be larger than F[7:0]									
											⁽³⁾ A delay time of $2 \times FrameFreq$ must be set if sending the command of 2Ch / 2Dh consecutively.									

3. Addressing Setting Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	00~0F	0	0	0	0	X ₃	X ₂	X ₁	X ₀	Set Lower Column Start Address for Page Addressing Mode	Set the lower nibble of the column start address register for Page Addressing Mode using X[3:0] as data bits. The initial display line register is reset to 0000b after RESET. Note (1) This command is only for page addressing mode
0	10~1F	0	0	0	1	X ₃	X ₂	X ₁	X ₀	Set Higher Column Start Address for Page Addressing Mode	Set the higher nibble of the column start address register for Page Addressing Mode using X[3:0] as data bits. The initial display line register is reset to 0000b after RESET. Note (1) This command is only for page addressing mode
0 0	20 A[1:0]	0 *	0 *	1 *	0 *	0 *	0 *	0 A ₁	0 A ₀	Set Memory Addressing Mode	A[1:0] = 00b, Horizontal Addressing Mode A[1:0] = 01b, Vertical Addressing Mode A[1:0] = 10b, Page Addressing Mode (RESET) A[1:0] = 11b, Invalid
0 0 0	21 A[7:0] B[7:0]	0 A ₇ B ₇	0 A ₆ B ₆	1 A ₅ B ₅	0 A ₄ B ₄	0 A ₃ B ₃	0 A ₂ B ₂	0 A ₁ B ₁	1 A ₀ B ₀	Set Column Address	Setup column start and end address A[7:0] : Column start address, range : 0-127d, (RESET=0d) B[7:0] : Column end address, range : 0-127d, (RESET =127d) Note (1) This command is only for horizontal or vertical addressing mode.
0 0 0	22 A[2:0] B[2:0]	0 * *	0 * *	1 * *	0 * *	0 * *	0 A ₂ B ₂	1 A ₁ B ₁	0 A ₀ B ₀	Set Page Address	Setup page start and end address A[2:0] : Page start Address, range : 0-7d, (RESET = 0d) B[2:0] : Page end Address, range : 0-7d, (RESET = 7d) Note (1) This command is only for horizontal or vertical addressing mode.
0	B0~B7	1	0	1	1	0	X ₂	X ₁	X ₀	Set Page Start Address for Page Addressing Mode	Set GDDRAM Page Start Address (PAGE0~PAGE7) for Page Addressing Mode using X[2:0]. Note (1) This command is only for page addressing mode

4. Hardware Configuration (Panel resolution & layout related) Command Table

D/C#Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0 40~7F	0	1	X ₅	X ₄	X ₃	X ₂	X ₁	X ₀	Set Display Start Line	Set display RAM display start line register from 0-63 using X ₅ X ₃ X ₂ X ₁ X ₀ . Display start line register is reset to 000000b during RESET.
0 A0/A1	1	0	1	0	0	0	0	X ₀	Set Segment Re-map	A0h, X[0]=0b: column address 0 is mapped to SEG0 (RESET) A1h, X[0]=1b: column address 127 is mapped to SEG0
0 A8 0 A[5:0]	1 *	0 *	1 A ₅	0 A ₄	1 A ₃	0 A ₂	0 A ₁	0 A ₀	Set Multiplex Ratio	Set MUX ratio to N+1 MUX N=A[5:0] : from 16MUX to 64MUX, RESET= 111111b (i.e. 63d, 64MUX) A[5:0] from 0 to 14 are invalid entry.
0 C0/C8	1	1	0	0	X ₃	0	0	0	Set COM Output Scan Direction	C0h, X[3]=0b: normal mode (RESET) Scan from COM0 to COM[N-1] C8h, X[3]=1b: remapped mode. Scan from COM[N-1] to COM0 Where N is the Multiplex ratio.
0 D3 0 A[5:0]	1 *	1 *	0 A ₅	1 A ₄	0 A ₃	0 A ₂	1 A ₁	1 A ₀	Set Display Offset	Set vertical shift by COM from 0d~63d The value is reset to 00h after RESET.
0 DA 0 A[5:4]	1 0	1 0	0 A ₅	1 A ₄	1 0	0 0	1 1	0 0	Set COM Pins Hardware Configuration	A[4]=0b, Sequential COM pin configuration A[4]=1b (RESET), Alternative COM pin configuration A[5]=0b (RESET), Disable COM Left/Right remap A[5]=1b, Enable COM Left/Right remap

5. Timing & Driving Scheme Setting Command Table

00	D5 A[7:0]	1 A ₇	1 A ₆	0 A ₅	1 A ₄	0 A ₃	1 A ₂	0 A ₁	1 A ₀	Set Display Clock Divide Ratio/Oscillator Frequency	A[3:0] : Define the divide ratio (D) of the display clocks (DCLK): Divide ratio= A[3:0] + 1, RESET is 0000b (divide ratio = 1) A[7:4] : Set the Oscillator Frequency, F _{osc} . Oscillator Frequency increases with the value of A[7:4] and vice versa. RESET is 1000b Range:0000b~1111b Frequency increases as setting value increases.												
00	D9 A[7:0]	1 A ₇	1 A ₆	0 A ₅	1 A ₄	1 A ₃	0 A ₂	0 A ₁	1 A ₀	Set Pre-charge Period	A[3:0] : Phase 1 period of up to 15 DCLK Clock 0 is invalid entry (RESET=2h) A[7:4] : Phase 2 period of up to 15 DCLK Clock 0 is invalid entry (RESET=2h)												
00	DB A[5:2]	1 0	1 0	0 A ₅	1 A ₄	1 A ₃	0 A ₂	1 0	1 0	Set V _{COMH} Deselect Level	<table><tr><th>A[5:2]</th><th>Hex code</th><th>V_{COMH} deselect level</th></tr><tr><td>0000b</td><td>00h</td><td>~ 0.64 x V_{CC}</td></tr><tr><td>1101b</td><td>34h</td><td>~ 0.78 x V_{CC} (RESET)</td></tr><tr><td>1111b</td><td>3Ch</td><td>~ 0.84 x V_{CC}</td></tr></table>	A[5:2]	Hex code	V _{COMH} deselect level	0000b	00h	~ 0.64 x V _{CC}	1101b	34h	~ 0.78 x V _{CC} (RESET)	1111b	3Ch	~ 0.84 x V _{CC}
A[5:2]	Hex code	V _{COMH} deselect level																					
0000b	00h	~ 0.64 x V _{CC}																					
1101b	34h	~ 0.78 x V _{CC} (RESET)																					
1111b	3Ch	~ 0.84 x V _{CC}																					

■ INITIALIZATION CODE

```
void InitOLED_MASTER_SSD1309(void)
```

```
{
    MainOLED_WCom(0xFD);    // SET COMMAND LOCK (012H 016H)
    MainOLED_WCom(0x12);
    MainOLED_WCom(0xAE);    //DOT MARTIX DISPLAY OFF
    MainOLED_WCom(0x81);    //CONTARST CONTROL(00H-0FFH)
    MainOLED_WCom(CONTRAST);
    MainOLED_WCom(0xA4);    //ENTIRE DISPLAY OFF(0A4H-0A5H)
    MainOLED_WCom(0xA6);    //SET NORMAL DISPLAY(0A6H-0A7H)

    MainOLED_WCom(0x00);    // SET LOW COLUMN START ADDRESS
    MainOLED_WCom(0x10);    //SET HIGH COLUMN START ADDRESS
    MainOLED_WCom(0x20);    //SET MEMORRY ADDRESSING MODE
    MainOLED_WCom(0x02);    //PAGE ADDRESSING MODE (RESET)
    MainOLED_WCom(0XB0);    // Set Page Start

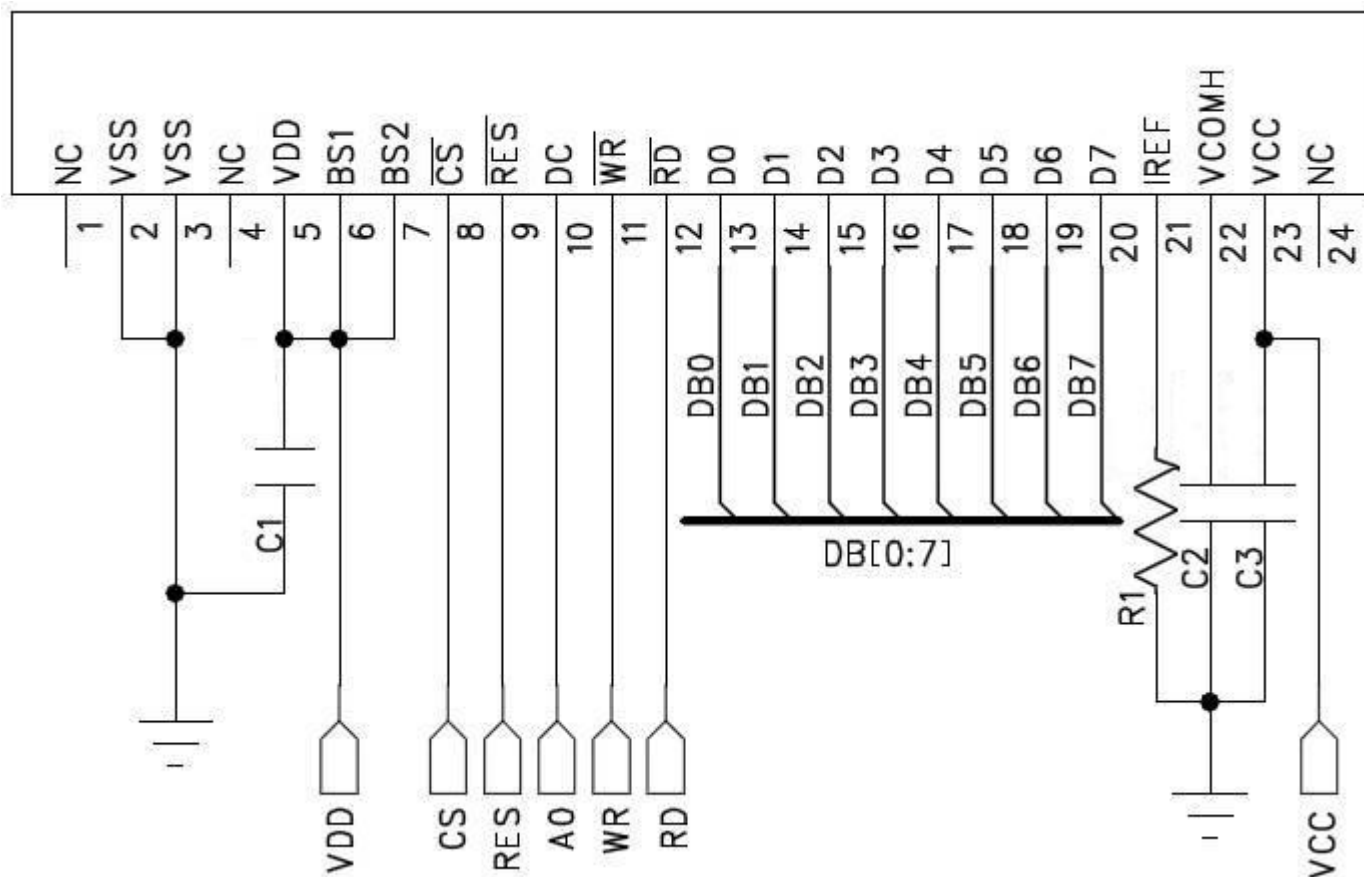
    MainOLED_WCom(0x40);    //SET DISPLAY STRART LINE (040H-07FH)
    MainOLED_WCom(0xA1);    //SET SEGMENT RE-MAP(0A0H-0A1H)
    MainOLED_WCom(0xA8);    //SET MULTIPLEX RATIO 64
    MainOLED_WCom(0x3F);
    MainOLED_WCom(0xC8);    //COM SCAN COM1-COM64(0C8H,0C0H)

    MainOLED_WCom(0xD3);    //SET DISPLAY OFFSET(OOH-3FH)
    MainOLED_WCom(0x00);
    MainOLED_WCom(0xDA);    //COM PIN CONFIGURATION
    MainOLED_WCom(0x12);
    MainOLED_WCom(0xD5);    //SET FRAME FREQUENCY
    MainOLED_WCom(0x80);
    MainOLED_WCom(0xD9);    //SET PRE_CHARGE PERIOD
    MainOLED_WCom(0x22);
    MainOLED_WCom(0xDB);    //SET VCOM DESELECT LEVEL
    MainOLED_WCom(0x34);

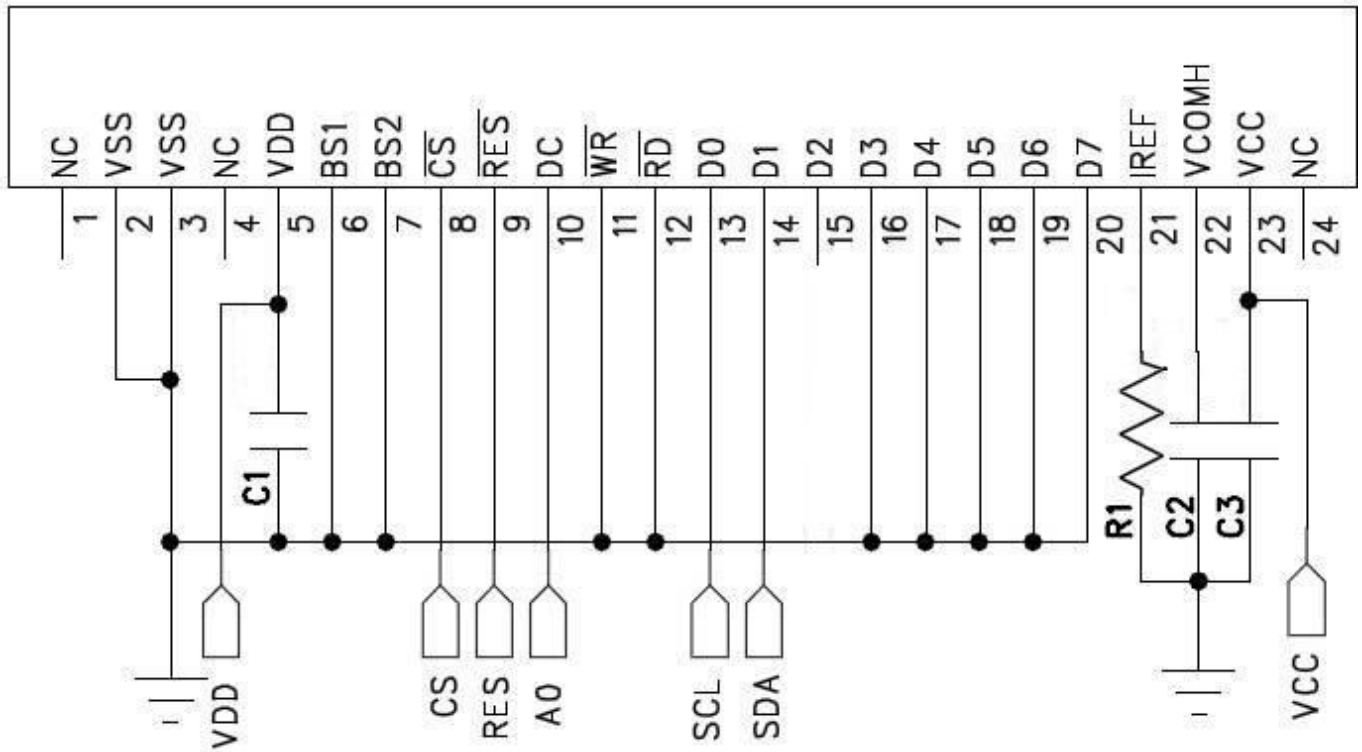
    MainOLED_WCom(0xAF);    //DSPLAY ON
}
```

■ SCHEMATIC EXAMPLE

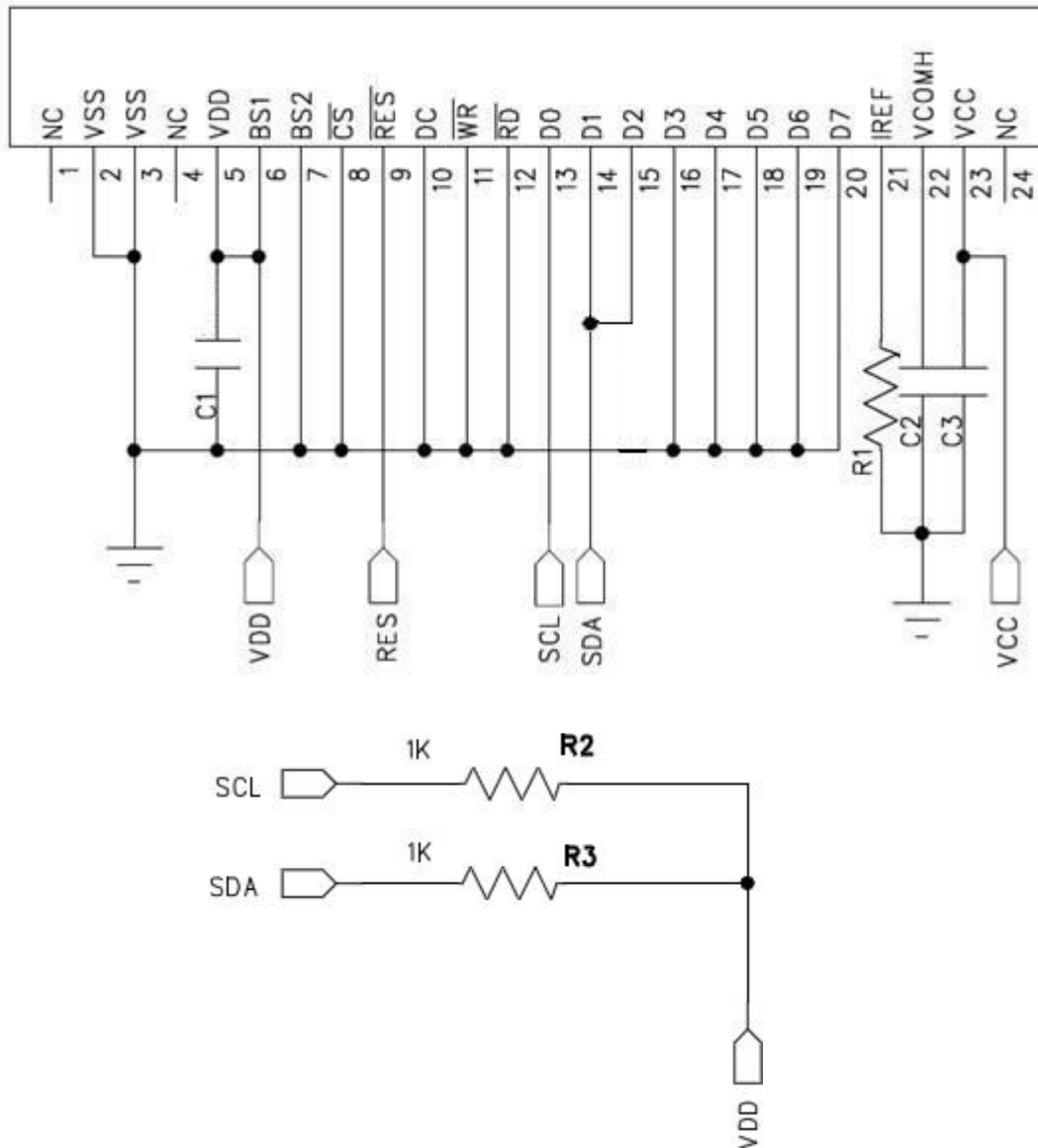
◆ 8080 Series Interface Application Circuit:



◆ Serial Interface Application Circuit:



◆ IIC Interface Application Circuit:



NOTE:

1. $R1 = (\text{Voltage at IREF} - VSS) / IREF \approx 910K\Omega$, $R2 = R3 = 1K\Omega$, $C1 = C2 = C3 = 4.7\mu F$;
2. The capacitor and the resistor value are recommended value. Select the appropriate value against module application.

■ RELIABILITY TESTS

Item		Condition	Criterion
High Temperature Storage (HTS)		85±2℃ , 200 hours	1. After testing, the function test is ok. 2. After testing, no addition to the defect. 3. After testing, the change of luminance should be within +/- 50% of initial value. 4. After testing, the change for the mono and area color must be within (+/-0.02, +/- 0.02) and for the full color it must be within (+/-0.04, +/-0.04) of initial value based on 1931 CIE coordinates. 5. After testing, the change of total current consumption should be within +/- 50% of initial value.
High Temperature Operating (HTO)		70±2℃ , 96 hours	
Low Temperature Storage (LTS)		-40±2℃ , 200 hours	
Low Temperature Operating (LTO)		-40±2℃ , 96 hours	
High Temperature / High Humidity Storage (HTHHS)		50±3℃ , 90%±3%RH, 120 hours	
Thermal Shock (Non-operation) (TS)		-20±2℃ ~ 25℃ ~ 70±2℃ (30min) (5min) (30min) 10cycles	
Vibration (Packing)	10~55~10Hz,amplitude 1.5mm, 1 hour for each direction x, y, z	1. One box for each test. 2. No addition to the cosmetic and the electrical defects.	
Drop (Packing)	Height : 1 m, each time for 6 sides, 3 edges, 1 angle		
ESD (finished product housing)	±4kV (R: 330Ω C: 150pF , 10times, air discharge)	1. After testing, cosmetic and electrical defects should not happen. 2. In case of malfunction or defect caused by ESD damage, it would be judged as a good part if it would be recovered to normal state after resetting.	

Note: 1) For each reliability test, the sample quantity is 3, and only for one test item.

2) The HTHHS test is requested the Pure Water(Resistance>10MΩ).

3) The test should be done after 2 hours of recovery time in normal environment.

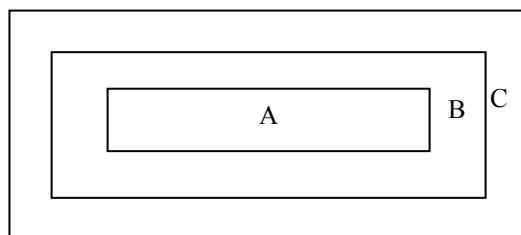
■ OUTGOING QUALITY CONTROL SPECIFICATION

◆ Standard

According to GB/T2828.1-2003/ISO 2859-1: 1999 and ANSI/ASQC Z1.4-1993,
General Inspection Level II.

◆ Definition

- 1 Major defect : The defect that greatly affect the usability of product.
- 2 Minor defect : The other defects, such as cosmetic defects, etc.
- 3 Definition of inspection zone:



Zone A: Active Area

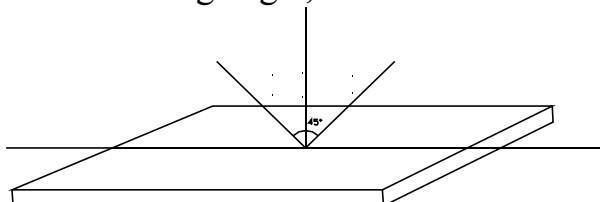
Zone B: Viewing Area except Zone A

Zone C: Outside Viewing Area

Note: As a general rule, visual defects in Zone C are permissible, when it is no trouble of quality and assembly to customer's product.

◆ Inspection Methods

- 1 The general inspection : under 20W x 2 or 40W fluorescent light, about 30cm viewing distance, within 45° viewing angle, under 25±5°C.



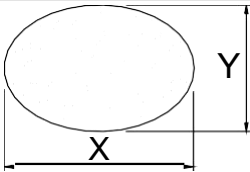
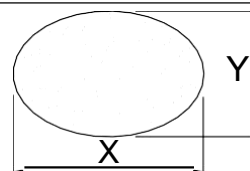
- 2 The luminance and color coordinate inspection : By PR705 or BM-7 or the equal equipments, in the dark room, under 25±5°C.

◆ Inspection Criteria

- 1 Major defect : AQL= 0.65

Item	Criterion
Function Defect	1. No display or abnormal display is not accepted
	2. Open or short is not accepted.
	3. Power consumption exceeding the spec is not accepted.
Outline Dimension	Outline dimension exceeding the spec is not accepted.
Glass Crack	Glass crack tends to enlarge is not accepted.

- 2 Minor Defect : AQL= 1.5

Item	Criterion			
Spot Defect (dimming and lighting spot)	Size (mm)		Accepted Qty	
			Area A + Area B	Area C
		$\Phi \leq 0.07$	Ignored	
		$0.07 < \Phi \leq 0.10$	3	Ignored
		$0.10 < \Phi \leq 0.15$	1	
		$0.15 < \Phi$	0	
Note : $\Phi = (x + y) / 2$				
Line Defect (dimming and lighting line)	L (Length) : mm	W (Width) : mm	Area A + Area B	Area C
	/	$W \leq 0.02$	Ignored	
	$L \leq 3.0$	$0.02 < W \leq 0.03$	2	Ignored
	$L \leq 2.0$	$0.03 < W \leq 0.05$	1	
	/	$0.05 < W$	As spot defect	
Remarks: The total of spot defect and line defect shall not exceed 4 pcs. The distance between two lines defects must exceed 1 mm				
Polarizer Stain	Stain which can be wiped off lightly with a soft cloth or similar cleaning is accepted, otherwise, according to the Spot Defect and the Line Defect.			
Polarizer Scratch	1. If scratch can be seen during operation, according to the criterions of the Spot Defect and the Line Defect.			
	2. If scratch can be seen only under non-operation or some special angle, the criterion is as below :			
	L (Length) : mm	W (Width) : mm	Area A + Area B	Area C
	/	$W \leq 0.02$	Ignore	
	$3.0 < L \leq 5.0$	$0.02 < W \leq 0.04$	2	Ignore
	$L \leq 3.0$	$0.04 < W \leq 0.06$	1	
/	$0.06 < W$	0		
Polarizer Air Bubble	Size		Area A + Area B	Area C
		$\Phi \leq 0.20$	Ignored	
		$0.20 < \Phi \leq 0.30$	2	Ignored
		$0.30 < \Phi \leq 0.50$	1	
		$0.50 < \Phi$	0	

Glass Defect (Glass Chipped)	1. On the corner	(mm)	<table><tr><td>x</td><td>≤ 1.5</td></tr><tr><td>y</td><td>≤ 1.5</td></tr><tr><td>z</td><td>$\leq t$</td></tr></table>	x	≤ 1.5	y	≤ 1.5	z	$\leq t$
	x	≤ 1.5							
	y	≤ 1.5							
	z	$\leq t$							
2. On the bonding edge	(mm)	<table><tr><td>x</td><td>$\leq a / 4$</td></tr><tr><td>y</td><td>$\leq s / 3 \ \&\leq 0.7$</td></tr><tr><td>z</td><td>$\leq t$</td></tr></table>	x	$\leq a / 4$	y	$\leq s / 3 \ \&\leq 0.7$	z	$\leq t$	
x	$\leq a / 4$								
y	$\leq s / 3 \ \&\leq 0.7$								
z	$\leq t$								
3. On the other edges	(mm)	<table><tr><td>x</td><td>$\leq a / 8$</td></tr><tr><td>y</td><td>≤ 0.7</td></tr><tr><td>z</td><td>$\leq t$</td></tr></table>	x	$\leq a / 8$	y	≤ 0.7	z	$\leq t$	
x	$\leq a / 8$								
y	≤ 0.7								
z	$\leq t$								
	Note: t: glass thickness ; s: pad width ; a: the length of the edge								
TCP Defect	Crack, deep fold and deep pressure mark on the TCP are not accepted								
Pixel Size	The tolerance of display pixel dimension should be within $\pm 20\%$ of the spec								
Luminance	Refer to the spec or the reference sample								
Color	Refer to the spec or the reference sample								

■ CAUTIONS IN USING OLED MODULE

◆ Precautions For Handling OLED Module:

1. OLED module consists of glass and polarizer. Pay attention to the following items when handling:
 - i. Avoid drop from high, avoid excessive impact and pressure.
 - ii. Do not touch, push or rub the exposed polarizers with anything harder than an HB pencil lead.
 - iii. If the surface becomes dirty, breathe on the surface and gently wipe it off with a soft dry cloth. If it is terrible dirty, moisten the soft cloth with Isopropyl alcohol or Ethyl alcohol. Other solvents may damage the polarizer. Especially water, Ketone and Aromatic solvents.
 - iv. Wipe off saliva or water drops immediately, contact the polarizer with water over a long period of time may cause deformation.
 - v. Please keep the temperature within specified range for use and storage.
Polarization degradation, bubble generation or polarizer peeling-off may occur with high temperature and high humidity.
 - vi. Condensation on the surface and the terminals due to cold or anything will damage, stain or dirty the polarizer, so make it clean as the way of iii.
2. Do not attempt to disassemble or process the OLED Module.
3. Make sure the TCP or the FPC of the Module is free of twisting, warping and distortion, do not pull or bend them forcefully, especially the soldering pins. On the other side, the SLIT part of the TCP is made to bend in the necessary case.
4. When assembling the module into other equipment, give the glass enough space to avoid excessive pressure on the glass, especially the glass cover which is much more fragile.
5. Be sure to keep the air pressure under 120 kPa, otherwise the glass cover is to be cracked.
6. Be careful to prevent damage by static electricity:
 - i. Be sure to ground the body when handling the OLED Modules.
 - ii. All machines and tools required for assembling, such as soldering irons, must be properly grounded.
 - iii. Do not assemble and do no other work under dry conditions to reduce the amount of static electricity generated. A relative humidity of 50%-60% is recommended.
 - iv. Peel off the protective film slowly to avoid the amount of static electricity generated.
 - v. Avoid to touch the circuit, the soldering pins and the IC on the Module by the body.
 - vi. Be sure to use anti-static package.
7. Contamination on terminals can cause an electrochemical reaction and corrode the terminal circuit, so make it clean anytime.
8. All terminals should be open, do not attach any conductor or semiconductor on the terminals.
9. When the logic circuit power is off, do not apply the input signals.
10. Power on sequence: $V_{DD} \rightarrow V_{CC}$, and power off sequence: $V_{CC} \rightarrow V_{DD}$.
11. Be sure to keep temperature, humidity and voltage within the ranges of the spec, otherwise shorten Module's life time, even make it damaged.
12. Be sure to drive the OLED Module following the Specification and datasheet of IC controller, otherwise something wrong may be seen.

13. When displaying images, keep them rolling, and avoid one fixed image displaying more than 30 seconds, otherwise the residue image is to be seen. This is the speciality of OLED.

◆ Precautions For Soldering OLED Module:

1. Soldering temperature : $260^{\circ}\text{C} \pm 10^{\circ}\text{C}$.
2. Soldering time : 3-4 sec.
3. Repeating time : no more than 3 times.
4. If soldering flux is used, be sure to remove any remaining flux after finishing soldering operation. (This does not apply in the case of a non-halogen type of flux.) It is recommended to protect the surface with a cover during soldering to prevent any damage due to flux spatters.

◆ Precautions For Storing OLED Module:

1. Be sure to store the OLED Module in the vacuum bag with dessicant.
2. If the Module can not be used up in 1 month after the bag being opened, make sure to seal the Module in the vacuum bag with dessicant again.
3. Store the Module in a dark place, do not expose to sunlight or fluorescent light.
4. The polarizer surface should not touch any other objects. It is recommended to store the Module in the shipping container.
5. It is recommended to keep the temperature between 0°C and 30°C , the relative humidity not over 60%.

◆ Limited Warranty

Unless relevant quality agreements signed with customer and law enforcement, for a period of 12 months from date of production, all products (except automotive products) HARESAN will replace or repair any of its OLED modules which are found to be functional defect when inspected in accordance with HARESAN OLED acceptance standards (copies available upon request). Cosmetic/visual defects must be returned to HARESAN within 90 days of shipment. Confirmation of such date should be based on freight documents. The warranty liability of HARESAN is limited to repair and/or replacement on the terms above. HARESAN will not be responsible for any subsequent or consequential events.

◆ Return OLED Module Under Warranty:

1. No warranty in the case that the precautions are disregarded.
2. Module repairs will be invoiced to the customer upon mutual agreement. Modules must be returned with sufficient description of the failures or defects.

◆ PRIOR CONSULT MATTER

1. For HARESAN standard products , we keep the right to change material ,process ... for improving the product property without any notice on our customer.
2. If you have special requirement about reliability condition, please let us know before you start the test on our samples.