Product Specification

7.0" TFT LCD Module

Model No :	**JWS070P3BLA27.V4**
Resolution:	1024*600
Interface:	LVDS 40PIN
Luminance:	500cd/m^2

< ◇> Preliminary Specification

< ◆> Finally Specification

CUSTOMER'S APPROVAL	
CUSTOMER :	
SIGNATURE:	**DATE:**

APPROVED BY	**PM REVIEWED**	**PD REVIEWED**	**PREPARED BY**

2. ABSOLUTE MAXIMUM RATINGS

The following are maximun values which, if exceeded, may cause faulty operation or damage to the unit.

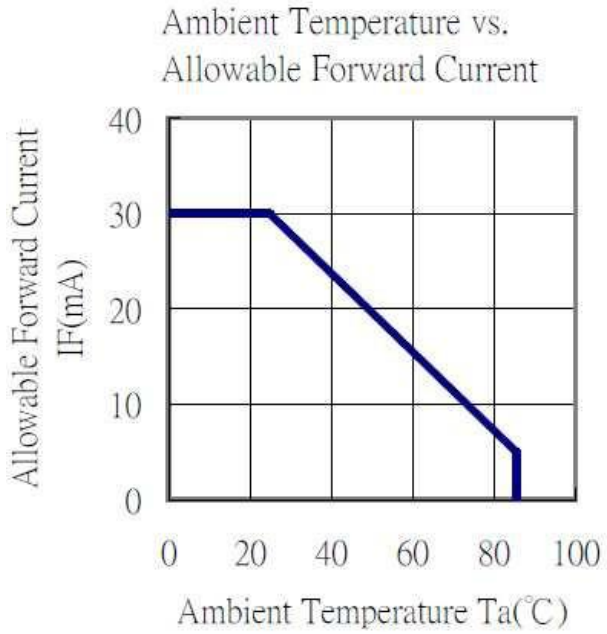
Item	Symbol	Min.	Max.	Unit	Note
Digital Supply Voltage	DVDD	-0.3	+3.96	V	
Analog Supply Voltage	AVDD	-0.5	+14.85	V	
Gate On Voltage	VGH	-0.3	+40	V	
Gate Off Voltage	VGL	-20	+0.3	V	
Gate On-Gate Off Voltage	VGH-VGL	12	40	V	
Signal Input Voltage	NIND0 ~ NIND3 PIND0 ~ PIND3 NINC,PINC	-0.5	5	V	
Forward Current （per LED）	If	-	30	mA	
Reverse Voltage（per LED）	VR	-	5	V	
Pulse forward currentn（per LED）	Ifp	-	60	mA	Note *2)
Operation Temperature (LCD panel surface overall)	T_{op1}	-20	80	℃	Note *1)
Operation Temperature	T_{op}	-20	70	℃	Note *1)
Storage Temperature	T_{stg}	-30	80	℃	Note *1)

Note：

*1) If the product were used out of the operation and storage range, it will have quality issue.

*2) Ifp Conditions ： Pulse Width≦10msec，Duty≦1/10.

*3) Each one of LED operation must be follow diagram of Ambient Temperature and Allowable Forward Current.



*4)If users use the product out off the environmemtal operation range（temperature and humidity）, it will

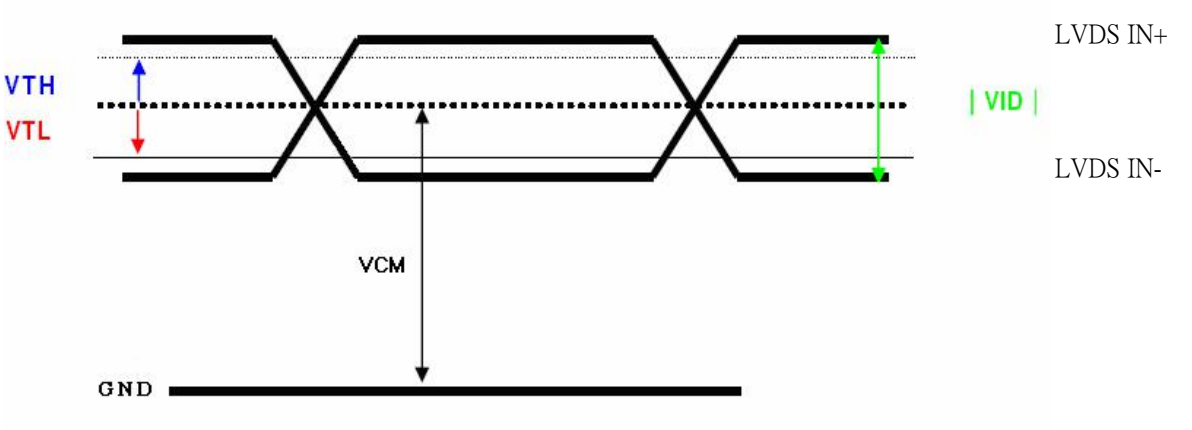
3. ELECTRICAL CHARACTERISTICS

3.1 Typical Operation Conditions

Ta=25℃

ITEM	SYMBOL	MIN	TYP	MAX	UNIT	NOTE
Digital Power Supply Voltage For LCD	DVDD	3	3.3	3.6	V	
Logic Input Voltage (LVDS:IN+,IN-)	VCM	$\frac{\lvert VID \rvert}{2}$	-	$2.4-\frac{\lvert VID \rvert}{2}$	V	Note1
	$\lvert VID \rvert$	200	-	600	mV	Note1
	VTH	-	-	100	mV	VCM=1.2V Note1
	VTL	-100	-	-	mV	
Analog Power Supply Voltage	AVDD	9.4	9.6	9.8	V	
Gate On Power Supply Voltage	VGH	17	18	19	V	
Gate Off Power Supply Voltage	VGL	-6.6	-6	-5.4	V	
Common Power Supply Voltage	VCOM	3.05	3.15	3.25	V	Note2
Logic Input Voltage	VIH	0.7*DVDD	-	DVDD	V	
	VIL	GND	-	0.3*DVDD	V	

Note1 :LVDS signal



Note2 :Please adjust VCOM to make the flicker level be minimum.

3.2 Current Consumption

ITEM	SYMBOL	CONDITION	MIN	TYPE	MAX	UNIT	NOTE
Gate On Power Current	IVGH	VGH =18V	- -	0.5	1	mA	Note1
Gate Off Power Current	IVGL	VGL= -6V	- -	0.5	1	mA	Note1
Digital Power Current	IDVDD	DVDD = 3.3V	- -	30	45	mA	Note1
Analog Power Current	IAVDD	AVDD = 9.0V	- -	35	45	mA	Note1
Total Power Consumption	PC		- -	447	604	mW	Note1

Note1: Typical: Under 256 gray pattern
Maximum: Under black pattern



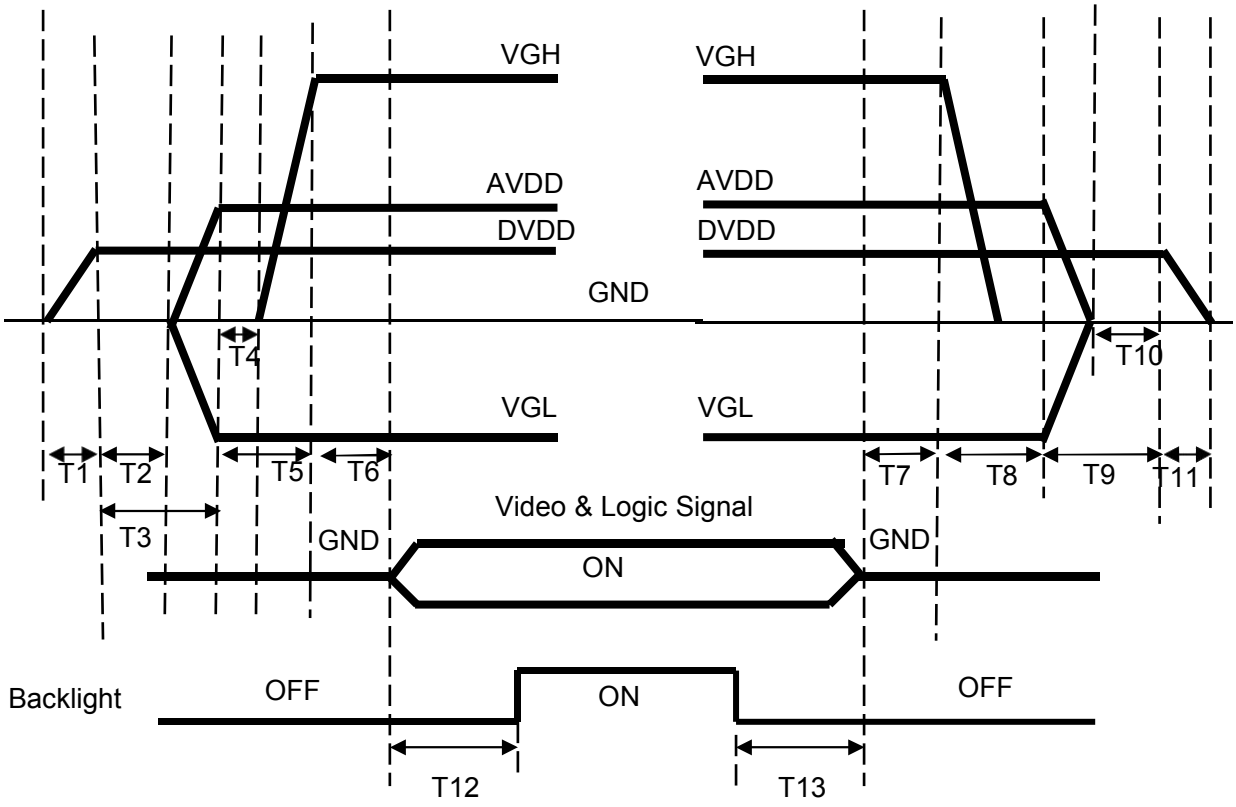
256 gray pattern



Black Pattern

3.3 Power、Signal Sequence

Power On：DVDD→AVDD/VGL →VGH →Video &Logic Signal→Backlight
Power Off：Backlight→Video &Logic Signal→ VGH→AVDD/VGL→DVDD



0<T1≦10ms
T2>0ms
T3>20ms
T4>0ms
T5>10ms
0<T6≦10ms
T12≧200ms

0ms<T7<50ms
0ms<T8<50ms
T9>0ms
T10>0ms
0<T11≦10ms
T13≧200ms

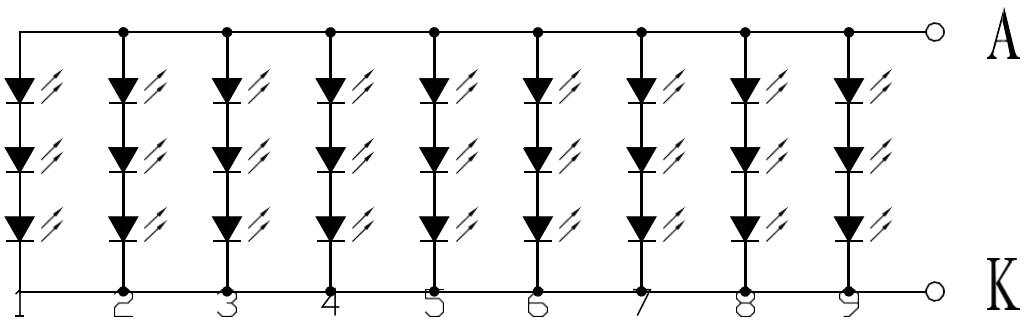
3.4 Backlight

Ta=25℃

ITEM	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	NOTE
LED current	IL	Ta=25℃ Each serial=20mA	180	200	-	mA	
LED voltage	VL	Ta=25℃ Each serial=20mA	9	9.9	10.5	V	
Power consumption	WL	Ta=25℃ Each serial=20mA	1.62	1.98	-	W	
LED Lifetime	-	Ta=25℃ Each serial=20mA	20000			Hr	

Note :

*1)LED Circuit Diagram：



*2) A：Anode(＋)，K：Cathode(－)

*3) Suggestion: Using the constant current control to avoid the leakage light and brightness quality issue.

*4) Definition of Led lifetime Luminance < Initial luminance 50%.

4. INTERFACE CONNECTION

4.1 CN1 (Input Signal)

Pin No.	Symbol	I/O	Function	Remark
1	VCOM	P	Common Voltage	
2	VDD	P	Power Voltage for digital circuit	
3	VDD	P	Power Voltage for digital circuit	
4	NC	---	No connection	
5	Reset	I	Global reset pin	
6	STBYB	I	Standby mode, Normally pulled high STBYB = “1”, normal operation STBYB = “0”, timing controller, source driver will turn off, all output are High-Z	
7	GND	P	Ground	
8	RXIN0-	I	- LVDS differential data input	
9	RXIN0+	I	+ LVDS differential data input	
10	GND	P	Ground	
11	RXIN1-	I	- LVDS differential data input	
12	RXIN1+	I	+ LVDS differential data input	
13	GND	P	Ground	
14	RXIN2-	I	- LVDS differential data input	
15	RXIN2+	I	+ LVDS differential data input	
16	GND	P	Ground	
17	RXCLKIN-	I	- LVDS differential clock input	
18	RXCLKIN+	I	+ LVDS differential clock input	
19	GND	P	Ground	
20	RXIN3-	I	- LVDS differential data input	
21	RXIN3+	I	+ LVDS differential data input	
22	GND	P	Ground	
23	NC	---	No connection	
24	NC	---	No connection	
25	GND	P	Ground	
26	NC	---	No connection	
27	DIMO	O	Backlight CABC controller signal output	
28	SELB	I	6bit/8bit mode select	Note1
29	AVDD	P	Power for Analog Circuit	
30	GND	P	Ground	
31	LED-	P	LED Cathode	
32	LED-	P	LED Cathode	
33	L/R	I	Horizontal inversion	Note3
34	U/D	I	Vertical inversion	Note3
35	VGL	P	Gate OFF Voltage	
36	CABCEN1	I	CABC H/W enable	Note2
37	CABCEN0	I	CABC H/W enable	Note2
38	VGH	P	Gate ON Voltage	
39	LED+	P	LED Anode	
40	LED+	P	LED Anode	

Remarks：

*1)if LVDS input data is 6bits,SELB must must be set to High
if LVDS input data is 8bit , SELB must be set to Low

5. INPUT SIGNAL(DE ONLY MODE)

5.1 Timing Specification

DE mode

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
DCLK frequency	fclk	40.8	51.2	67.2	MHz
Horizontal display area	thd		1024		DCLK
HSD period	th	1114	1344	1400	DCLK
HSD blanking	thb+thfp	90	320	376	DCLK
Vertical display area	tvd		600		T_H
VSD period	tv	610	635	800	T_H
VSD blanking	tvbp+tvfp	10	35	200	T_H

DE mode (1024x600)

HV mode

- **Horizontal timing**

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
DCLK frequency	fclk	44.9	51.2	63	MHz
Horizontal display area	thd		1024		DCLK
HSD period	th	1200	1344	1400	DCLK
HSD pulse Width	thpw	1	-	140	DCLK
HSD back porch	thbp		160		DCLK
HSD front porch	thfp	16	160	216	DCLK

HV mode horizontal timing (1024x600)

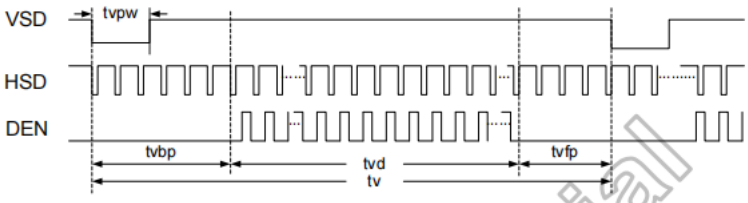
- **Vertical timing**

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Vertical display area	tvd		600		T_H
VSD period	tv	624	635	750	T_H
VSD pulse width	tvpw	1	-	20	T_H
VSD back porch	tvbp		23		T_H
VSD front porch	tvfp	1	12	127	T_H

HV mode vertical timing (1024x600)

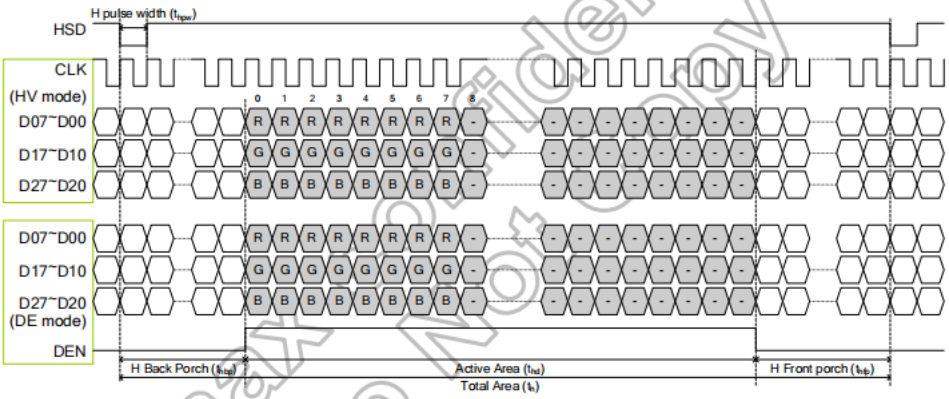
5.2 Timing sequence(Timing chart)

- **Vertical timing**



Vertical input timing diagram

- **Horizontal timing**



Horizontal input timing diagram

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