

Chapter 1 Introduction

1.1 Overview

RK3308 is a high-performance Quad-core application processor designed for intelligent voice interaction, audio input/output processing, and other digital multimedia applications. Embedded rich audio interfaces, such as I2S, PCM, TDM, PDM, SPDIF, HDMI ARC and so on, can meet different audio application development, reduce hardware development complexity and development cost.

Embedded Voice Activity Detection function will monitor human voice at any time, respond to human voice request timely and fast setup intelligent voice interaction application, which will also reduce hardware system power consumption and improve battery endurance.

RK3308 has high-performance external memory interface (DDR2/DDR3/DDR3L/LPDDR2) capable of sustaining demanding memory bandwidths.

1.2 Features

The features listed below which may or may not be present in actual product, may be subject to the third party licensing requirements. Please contact Rockchip for actual product feature configurations and licensing requirements.

1.2.1 Microprocessor

- Quad-core ARM Cortex-A35 CPU
- ARM architecture v8-A instruction set
- ARM Neon Advanced SIMD (single instruction, multiple data) support for accelerated media and signal processing computation
- ARMv8 Cryptography Extensions
- 256KB unified system L2 cache
- Include VFP v4 hardware to support single and double-precision operations
- Integrated 32KB L1 instruction cache, 32KB L1 data cache with 4-way set associative
- TrustZone technology support
- Separate power domains for CPU core system to support internal power switch and externally turn on/off based on different application scenario
 - PD_A35_0: 1st Cortex-A35 + Neon + FPU + L1 I/D Cache
 - PD_A35_1: 2nd Cortex-A35 + Neon + FPU + L1 I/D Cache
 - PD_A35_2: 3rd Cortex-A35 + Neon + FPU + L1 I/D Cache
 - PD_A35_3: 4th Cortex-A35 + Neon + FPU + L1 I/D Cache
- One isolated voltage domain to support DVFS

1.2.2 Memory Organization

- Internal on-chip memory
 - BootROM
 - Internal SRAM
- External off-chip memory^①
 - DDR2/DDR3/DDR3L/LPDDR2
 - 8bits Asynchronism Nand Flash
 - eMMC
 - SPI Nor/Nand Flash
 - SD Card

1.2.3 Internal Memory

- Internal BootRom
 - Support system boot from the following device:
 - ◆ Asynchronism Nand Flash
 - ◆ eMMC interface
 - ◆ SPI Flash interface

- ◆ SDMMC interface
- Support system code download by the following interface:
 - ◆ USB OTG interface (Device mode)
- Internal SRAM
 - Size: 256KB

1.2.4 External Memory or Storage device

- Dynamic Memory Interface (DDR2/DDR3/DDR3L/LPDDR2)
 - Compatible with JEDEC standards
 - Compatible with DDR2-1066/DDR3-1600/DDR3L-1600/LPDDR2-1066
 - Support 16-bit data width
 - Support 1 ranks (chip selects)
 - Support max 512MB addressing space
 - Low power modes, such as power-down and self-refresh for SDRAM
- Nand Flash Interface
 - Support Asynchronism Nand flash
 - Data bus width is 8bits
 - Support 1 chip select
 - Up to 16bits/1KB hardware ECC
- eMMC Interface
 - Compatible with standard INAND interface
 - Compatible with eMMC specification 4.41, 4.51, 5.0 and 5.1
 - Support three data bus width: 1-bit, 4-bit or 8-bit
 - Support up to HS200; but not support CMD Queue
- Serial Flash Interface
 - Support transfer data from/to SPI flash device
 - Support x1,x2,x4 data bits mode
 - Support up to 1 chip select
- SD/MMC Interface
 - Compatible with SD3.0, MMC ver4.51
 - Data bus width is 4bits

1.2.5 System Component

- CRU (clock & reset unit)
 - One oscillator with 24MHz clock input
 - Support clock gating control for individual components
 - Support global soft-reset control for whole chip, also individual soft-reset for each component
- PMU(power management unit)
 - 2 separate voltage domains(CORE_VDD/LOGIC_VDD)
 - 4 separate cpu power domains, which can be power up/down by software based on different application scenes
 - Multiple configurable work modes to save power by different frequency or automatic clock gating control or power domain on/off control
- Timer
 - Six 64bits timers with interrupt-based operation for non-secure application
 - Six 64bits timers with interrupt-based operation for secure application
 - Support two operation modes: free-running and user-defined count
 - Support timer work state checkable

- PWM
 - Four on-chip PWMs(PWM0~PWM3) with interrupt-based operation
 - Programmable pre-scaled operation to bus clock and then further scaled
 - Embedded 32-bit timer/counter facility
 - Support capture mode
 - Provides reference mode and output various duty-cycle waveform
 - Support continuous mode or one-shot mode
 - Optimized for IR application for PWM3
- Watchdog
 - 32-bit watchdog counter
 - Counter counts down from a preset value to 0 to indicate the occurrence of a timeout
 - WDT can perform two types of operations when timeout occurs:
 - ◆ Generate a system reset
 - ◆ First generate an interrupt and if this is not cleared by the service routine by the time a second timeout occurs then generate a system reset
 - Programmable reset pulse length
 - Totally 16 defined-ranges of main timeout period
- Interrupt Controller
 - Support 4 PPI interrupt source and 89 SPI interrupt sources input from different components
 - Support 16 software-triggered interrupts
 - Two interrupt outputs (nFIQ and nIRQ) separately for each Cortex-A35, both are low-level sensitive
 - Support different interrupt priority for each interrupt source, and they are always software-programmable
- DMAC
 - Micro-code programming based DMA
 - The specific instruction set provides flexibility for programming DMA transfers
 - Linked list DMA function is supported to complete scatter-gather transfer
 - Support internal instruction cache
 - Embedded DMA manager thread
 - Support data transfer types with memory-to-memory, memory-to-peripheral, peripheral-to-memory
 - Signals the occurrence of various DMA events using the interrupt output signals
 - Mapping relationship between each channel and different interrupt outputs is software-programmable
 - Two embedded DMA controllers for peripheral system
 - DMAC0 features,
 - ◆ 6 channels in total
 - ◆ 10 hardware request from peripherals
 - ◆ 2 interrupt output
 - ◆ Dual APB slave interface for register configuration, designated as secure and non-secure
 - ◆ Support TrustZone technology and programmable secure state for each DMA channel
 - DMAC1 features,
 - ◆ 8 channels in total
 - ◆ 20 hardware request from peripherals
 - ◆ 2 interrupt output
 - ◆ Dual APB slave interface for register configuration, designated as secure and non-secure
 - ◆ Support TrustZone technology and programmable secure state for each DMA channel

- Trust Execution Environment system
 - Support TrustZone technology for the following components
 - ◆ Cortex-A35, support secure and non-secure mode, switch by software
 - ◆ System general DMAC, support dedicated channels work only in secure mode
 - ◆ Secure OTP, only can be accessed by Cortex-A35 in secure mode and secure key reader block
 - ◆ Internal SRAM, part of space is addressed only in secure mode, detailed size is software-programmable together with TZMA (TrustZone memory adapter)
 - ◆ Firewall is embedded to manage the other master/slave function components
 - Cipher engine
 - ◆ Support SHA-1, SHA-256/224, SHA-512/384, MD5 with hardware padding
 - ◆ Support HMAC of SHA-1, SHA-256, SHA-512, MD5 with hardware padding
 - ◆ Support AES-128, AES-192, AES-256 encrypt & decrypt cipher
 - ◆ Support DES & TDES cipher
 - ◆ Support AES ECB/CBC/OFB/CFB/CTR/CTS/XTS/CCM/GCM/CBC-MAC/CMAC mode
 - ◆ Support DES/TDES ECB/CBC/OFB/CFB mode
 - ◆ Support up to 4096 bits PKA mathematical operations for RSA/ECC
 - Support data scrambling for DDR2/DDR3/DDR3L/LPDDR2
 - Support up to 256 bits TRNG output
 - Support secure OTP
 - Support secure debug
 - Support secure OS

1.2.6 Video Output Processor (VOP)

- Display Interface
 - Support parallel RGB LCD output interface
 - ◆ 18-bit(RGB666)
 - ◆ 16-bit(RGB565)
 - Support MCU interface
 - Max output resolution is 1080p
- Display process
 - Background layer: programmable 24-bit color
 - Win0 layer
 - ◆ RGB888, ARGB888, RGB565, YCbCr422, YCbCr420, YCbCr444
 - ◆ RB/alpha/mid/uv swap
 - ◆ 1/8 to 8 scaling-down and scaling-up engine
 - ◆ Support virtual display
 - ◆ 256 level alpha blending (pre-multiplied alpha support)
 - ◆ Transparency color key
 - ◆ YCbCr2RGB(rec601-mpeg/ rec601-jpeg/rec709)
 - ◆ RGB2YCbCr(BT601/BT709)
 - Win1 layer
 - ◆ RGB888, ARGB888, RGB565
 - ◆ RB/alpha/endian swap
 - ◆ Support virtual display
 - ◆ 256 level alpha blending (pre-multiplied alpha support)
 - ◆ Transparency color key
 - ◆ RGB2YCbCr(BT601/BT709)
- Others
 - Win0 layer and Win1 layer overlay exchangeable
 - BCSH(Brightness, Contrast, Saturation, Hue adjustment)
 - BCSH: YCbCr2RGB(rec601-mpeg/rec601-jpeg/rec709)
 - BCSH: RGB2YCbCr(BT601/BT709)
 - Support Gamma adjust for PAD
 - Support dither down allegro RGB888to666 RGB888to565 & dither down frc

- Support programmable data sampling sensibility, rising or falling edge
- TDM with 8 channel
 - Support 4 TDM_8CH, share same I2S_8CH controller accordingly
 - Support I2S normal, left and right justified mode serial audio data transfer
 - Support PCM normal, 1/2 cycle left shift, 1 cycle left shift, 3/2 cycle left shift, 2 cycle left shift mode serial audio data transfer
 - Support TDM programmable slot bit width: 16~32bits
 - Support TDM programmable frame width: 32~512bits
 - Support TDM programmable FSYNC width
 - Sample rate up to 192KHz@2CH and 48KHz@8CH
 - Support DMA transfer
 - Support separate transmit and receive DMA request mode
 - Support 1 common SCLK signal for receiving and transmitting
 - Support 2 independent SCLK signals for receiving and transmitting
 - Support 1 common LRCK signal for receiving and transmitting
 - Support 2 independent LRCK signals for receiving and transmitting
 - Support configurable SCLK and LRCK polarity
- SPDIF
 - Support SPDIF TX x 1
 - Support SPDIF RX x 1
 - Support HDMI ARC
 - Support 16bits/20bits/24bits resolution
 - Support DMA transfer
 - Support linear PCM mode (IEC-60958)
 - Support non-linear PCM transfer(IEC-61937)
 - Sample rate up to 192KHz
 - Support SPDIF RX is bypassed to SPDIF TX directly
- Voice Activity Detection(VAD)
 - Support single Mic human voice detection
 - Support human voice frequency band filtering
 - Support human voice amplitude detection
 - Support Muti-Mic array data store before voice detection event or after voice detection event two modes, and also can support Muti-Mic array data is not stored in voice detection process
 - Support Mic data from Analog Mic, I2S Digital Mic or PDM digital Mic
 - Store memory is shared with system internal memory
- Embedded Audio Codec
 - 24 bit DAC which support stereo headphone out and line out
 - 24 bit ADC which support max 8 channel microphone input and 2 channel line in
 - Support differential microphone input and can also be configured as single-end
 - Support Po=18mW for 16ohm and 9mW for 32ohm headphone output
 - Support Automatic Level Control (ALC)
 - Support programmable input/output analog gains
 - Support two programmable microphone bias. The max programmable voltage can reach to $0.85 \times AVDD3V3$
 - Support I2S as the digital signal interface for both ADC and DAC
 - Support both master and slave mode
 - Support 16bits/24bits resolution
 - Support I2S normal, left and right justified mode
 - Support sample rate,
 - ◆ Group1: 8khz,16khz,32kHz,64kHz,128khz
 - ◆ Group2: 11.025khz,22.05khz,44.1khz,88.2khz,176.4khz
 - ◆ Group3: 12khz,24khz,48khz,96khz,192khz
 - ◆ Support ADC/DAC sample rate any combination of group1/group2/group3

- Support headphone jack detection input

1.2.8 Connectivity

- SDIO interface
 - Compatible with SDIO3.0 protocol
 - 4bits data bus widths
- MAC 10/100 Ethernet Controller
 - Supports 10/100-Mbps data transfer rates with the RMI interfaces
 - Supports both full-duplex and half-duplex operation
 - Supports IEEE 802.1Q VLAN tag detection for reception frames
 - Support detection of LAN wake-up frames and AMD Magic Packet frames
 - Handles automatic retransmission of Collision frames for transmission
- USB 2.0 OTG
 - Compatible with USB 2.0 specification
 - Supports high-speed(480Mbps), full-speed(12Mbps) and low-speed(1.5Mbps) mode
- USB 2.0 Host
 - Compatible with USB 2.0 specification
 - Supports high-speed(480Mbps), full-speed(12Mbps) and low-speed(1.5Mbps) mode
 - Support Enhanced Host Controller Interface Specification (EHCI), Revision 1.0
 - Support Open Host Controller Interface Specification (OHCI), Revision 1.0a
- SPI interface
 - Support three SPI Controller(SPI0/SPI1/SPI2)
 - Support one chip-select for each SPI Controller
 - Support serial-master and serial-slave mode, software-configurable
- I2C interface
 - Support four I2C interface(I2C0/I2C1/I2C2/I2C3)
 - Support 7bits and 10bits address mode
 - Software programmable clock frequency
 - Data on the I2C-bus can be transferred at rates of up to 100 kbit/s in the Standard-mode, up to 400 kbit/s in the Fast-mode or up to 1 Mbit/s in Fast-mode Plus
- UART Controller
 - Support five UART interface(UART0/UART1/UART2/UART3/UART4)
 - Embedded two 64-byte FIFO for TX and RX operation respectively
 - Support 5bit,6bit,7bit,8bit serial data transmit or receive
 - Standard asynchronous communication bits such as start, stop and parity
 - Support different input clock for UART operation to get up to 4Mbps baud rate
 - Support auto flow control mode for UART0/UART1/UART4

1.2.9 Others

- Multiple group of GPIO
 - All of GPIOs can be used to generate interrupt
 - Support level trigger and edge trigger interrupt
 - Support configurable polarity of level trigger interrupt
 - Support configurable rising edge, falling edge and both edge trigger interrupt
 - Support configurable pull direction(pullup or pulldown)
 - Support configurable drive strength
- Temperature Sensor(TS-ADC)
 - Up to 50KS/s sampling rate
 - Support two temperature sensor
 - -20~120℃ temperature range and 5℃ temperature resolution