

JiAXUN

佳 迅 智 能 科 技

Jiaxun PLC Module JMN-L80A Specification



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JiAXUN INTELLIGENT TECHNOLOGY LIMITED

Content

A. Product Introduction	1
B. Product Features	2
C. Technical Parameters	4
D. Pin Definition	4
E. Module Package Size	11
F. Hardware Design Description	12
G. Disclaimer	15

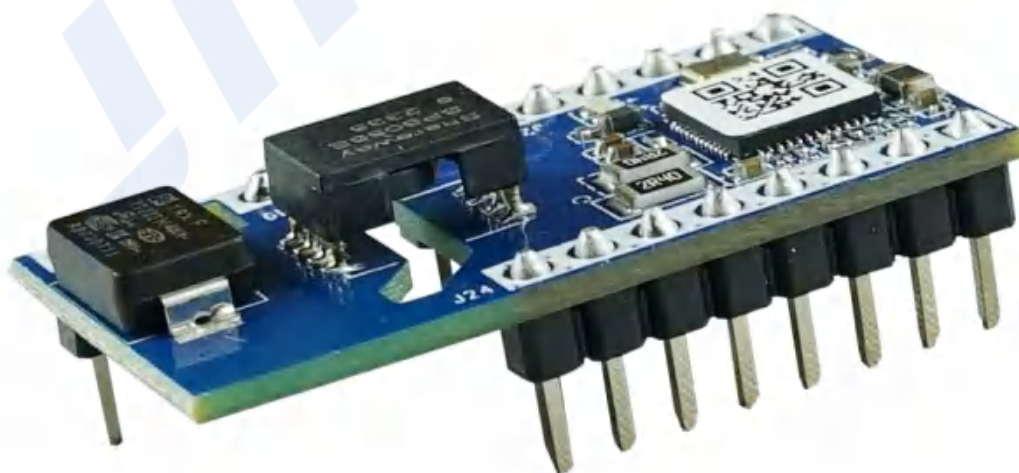


A. Product Introduction

The JMN-L80A is a highly integrated, ultra-compact PLC communication module designed for simplified wiring and space-saving deployment. It is widely applicable in real-time PLC communication scenarios such as smart street lighting, smart home systems, intelligent parking, central air conditioning, and IoT terminal devices in ubiquitous power networks.

- **High-Performance Chip:** Built on the PS0211 chip, integrating a multi-mode (high-speed/low-speed) PLC modem and an ARM Cortex-M3 processor.
- **Standards Compliance:** Supports IEEE P1901.1 standards with OFDM/FSK modulation, featuring tonemask and SunSpec standard compatibility.
- **Versatile Interfaces:** Offers multiple peripheral interfaces including UART, PWM, GPIO, ADC, SPI, and I2C for flexible development.
- **Integrated Design:** Incorporates a built-in Line-Driver to enhance signal transmission reliability.
- **Developer Support:** Provides an open development environment and a secure, efficient operating system for rapid deployment.

Note: This document is intended for hardware development engineers, hardware test engineers, and technical support engineers.



B. Product Features

1) CPU & Memory Performance

- High-performance Cortex-M3 processor running at 200MHz.
- Embedded 256KB SRAM and 512KB Flash for efficient data processing and storage.

2) PHY Layer Features

- Compliant with a subset of IEEE 1901.1 standard, ensuring interoperability with compatible chips.
- Supports dual frequency bands: 0.5-3.7MHz and 2.5-5.7MHz, configurable via software.
- Utilizes OFDM technology with BPSK/QPSK modulation.
- Features FEC (Forward Error Correction) and CRC (Cyclic Redundancy Check) for robust noise immunity and error correction.

3) MAC Layer Features

- Supports TDMA (Time Division Multiple Access) and CSMA/CA (Carrier Sense Multiple Access/Collision Avoidance) for optimized channel access.
- Enables data segmentation and reassembly to improve transmission efficiency.
- Implements data retransmission for reliable communication.
- Offers 4-level QoS (Quality of Service) to prioritize diverse traffic.

4) Networking Capabilities

- Fast auto-networking: Establishes 200-node, 2-tier networks within 10 seconds.
- Supports dynamic routing and multi-path addressing.
- Compatible with unicast, multicast, and broadcast communication modes.

5) Peripheral Interfaces

- Provides UART, GPIO, SPI, I2C, PWM output, and ADC input interfaces.

6) Communication Metrics

- PHY layer peak rate: 0.507Mbps | Application layer rate: 80Kbps.
- Transmit power: Built-in Line Driver with up to -51dBm/Hz.
- Receiver sensitivity: -98dBm (lab-tested at 30% packet reception rate).

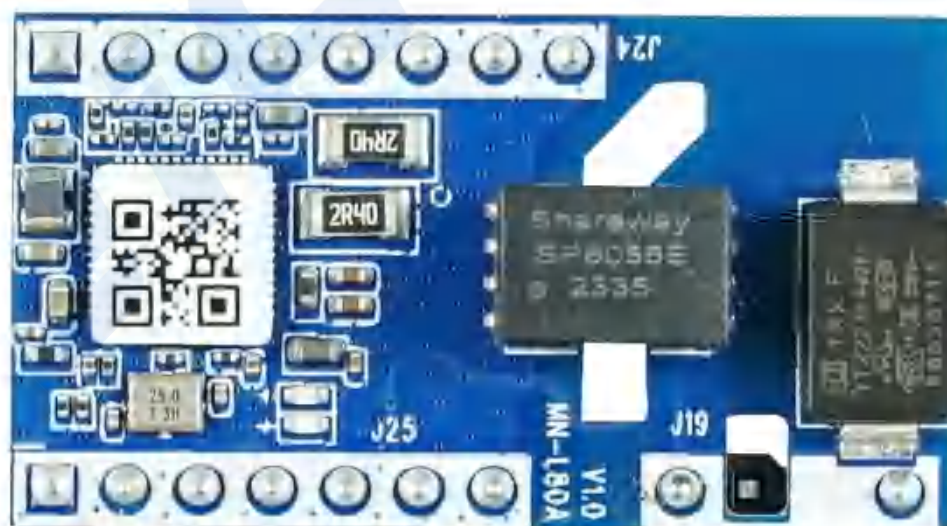


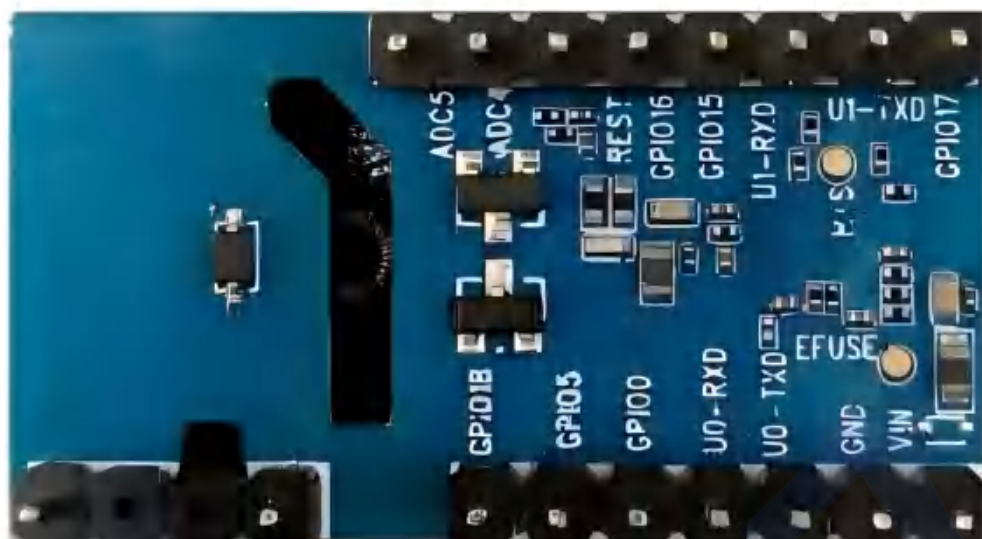
C. Technical Parameters

Module Name	JMN-L80A
Main Interfaces	UART, PWM, GPIO, ADC, SPI, I2C
Communication Methods	Power line communication, supports OFDM/FSK modulation
PCB Size	33.0mm*18.0mm*5.8±0.3mm (Pin Height: 8mm)
Static Power Consumption	≤ 0.15W (networking without packet sending)
Dynamic Operating Power	≤ 0.5W
Operating Voltage	3.3±0.3V DC
Operating Temperature	-40°C ~ +85°C
Storage Temperature	-40°C ~ +125°C

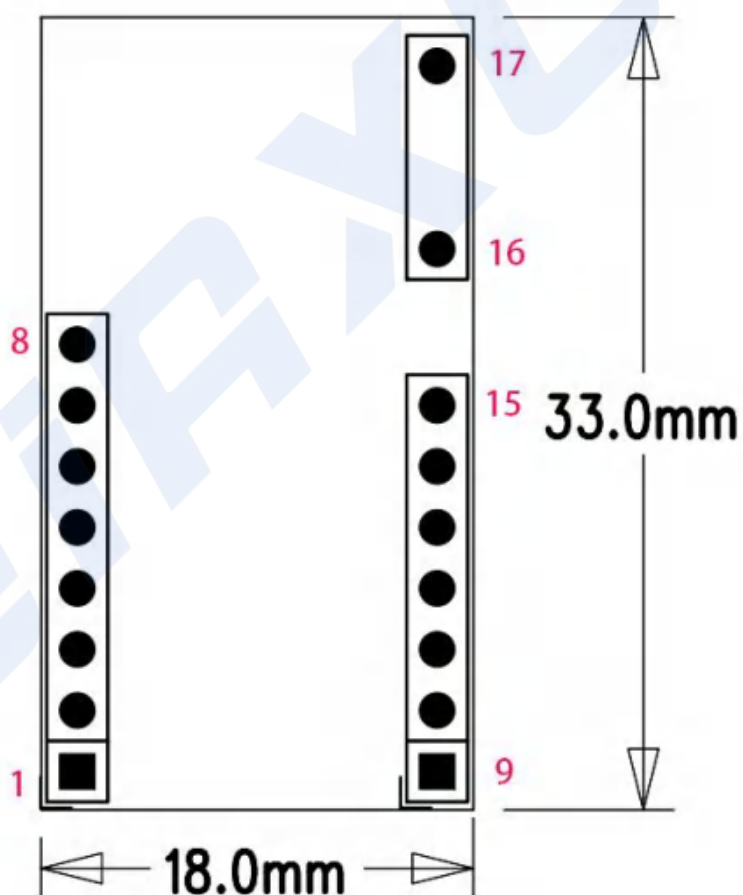
D. Pin Definition

1) Module Appearance





2) Pin Block Diagram



3) Pin Definition and Multiplexing Instructions

NO.	Pin Name	Description
1	GPIO17	Multipurpose GPIO pin Alternate Function 0: GPIO_17 (Default: Input/Output) Alternate Function 1: SSP_DLSPi Data Input Alternate Function 2: SSP_DGSPi Data Output
2	UART1_TXD	UART1/GPIO14 multiplexed pin (Default: 10K Ω pull-down) Alternate Function 0: UART1_TX (Primary use: User port selection, software configuration, network testing) Alternate Function 1: GPIO_14 (General Purpose I/O) Alternate Function 5: DC_SCL (I2C Clock)
3	UART1_RXD	UART1/GPIO13 multiplexed pin (Default: 10K Ω pull-up) Alternate Function 0: UART1_RX (Primary use: Software configuration, network testing) Alternate Function 1: GPIO_13 (General Purpose I/O) Alternate Function 5: DC_SDA (I2C Data)
4	GPIO15	Alternate Function 0: GPIO15 (Default: Input/Output) Alternate Function 1: SPI_CK (SPI Clock Input)
5	GPIO16	Alternate Function 0: GPIO16 (Default: Input/Output) Alternate Function 1: SPI_CS (SPI Chip Select, Active Low)
6	RESET	PLC Reset Input (Internal pull-up) Software Reset Control: A low pulse ($\leq 5\text{ms}$) during normal operation triggers PS0211 reset. Must remain stable during operation (recommend single-point connection).
7	ADC4	ADC Input (Voltage Range: 0.1V-2.75V)
8	ADC5	ADC Input (Voltage Range: 0.1V-2.75V)
9	3.3Vin	Module Power Supply (3.3V) Operating Range: 3.0-3.6V (Ripple <3%), Current Requirement: $\geq 200\text{mA}$



10	GND	System Ground
11	UART0_TXD	UART0/GPIO multiplexed pin (Default: 10KΩ pull-down when connected to external MCU. Primary use: Upper-layer MCU communication via UART0) Alternate Function 0: GPIO_10 (Default: Input/Output) Alternate Function 1: UART0_TXD (UART0 Data Transmission)
12	UART0_RXD	UART0/GPIO multiplexed pin (Default: 10KΩ pull-down when connected to external MCU. Primary use: Upper-layer MCU communication via UART0) Alternate Function 0: GPIO_9 (Default: Input/Output) Alternate Function 1: UART0_RXD (UART0 Data Reception)
13	PWM0/GPIO0	PWM/GPIO multiplexed pin (Default: PWM mode with internal 10KΩ pull-down) Alternate Function 0: GPIO_0 (Default: Input/Output) Alternate Function 1: LED4 (General-purpose LED) Alternate Function 3: PWM_OUT (Pulse Width Modulation output)
14	PWM1/GPIO5	PWM/GPIO multiplexed pin (Default: PWM mode with internal 10KΩ pull-down) Alternate Function 0: GPIO_5 (Default: Input/Output) Alternate Function 3: PWM1_OUT (Pulse Width Modulation output)
15	GPIO18	Multipurpose GPIO pin Alternate Function 0: GPIO18 (Default: Input/Output) Alternate Function 1: SPI_DO (SPI Data Output) Alternate Function 2: SPI_DI (SPI Data Input)
16	L	220V AC Live Line (Communication port) Requires filter network design for AC power isolation Standard protection rating: Differential/Common mode: $\pm 4\text{KV}$
17	N	220V AC Neutral Line (Communication port) Requires filter network design for AC power isolation

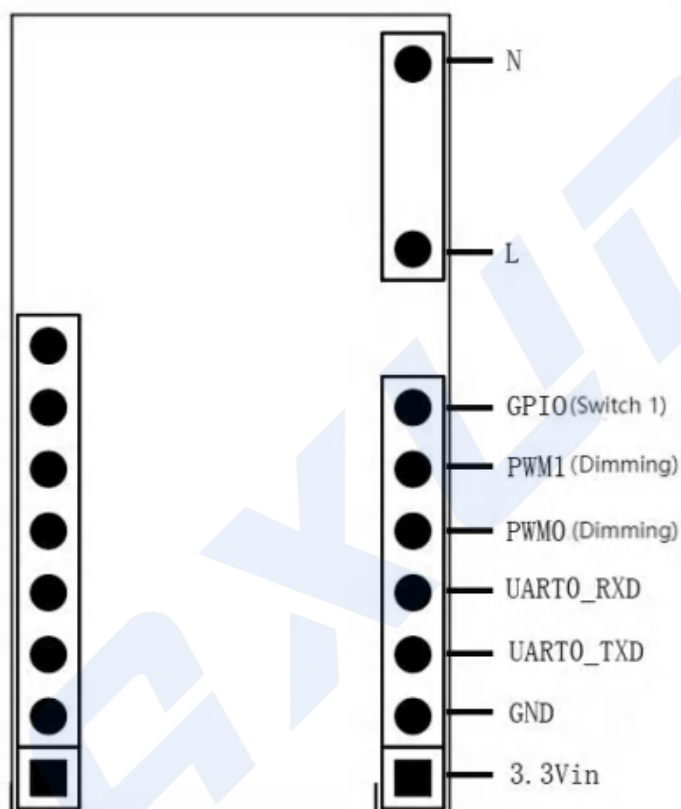


		Standard protection rating: Differential/Common mode: $\pm 4\text{KV}$
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1) Single-Port Interface Application Recommendation

Recommended Model: JMN-L80A-W (90° right-angle pin header, single-

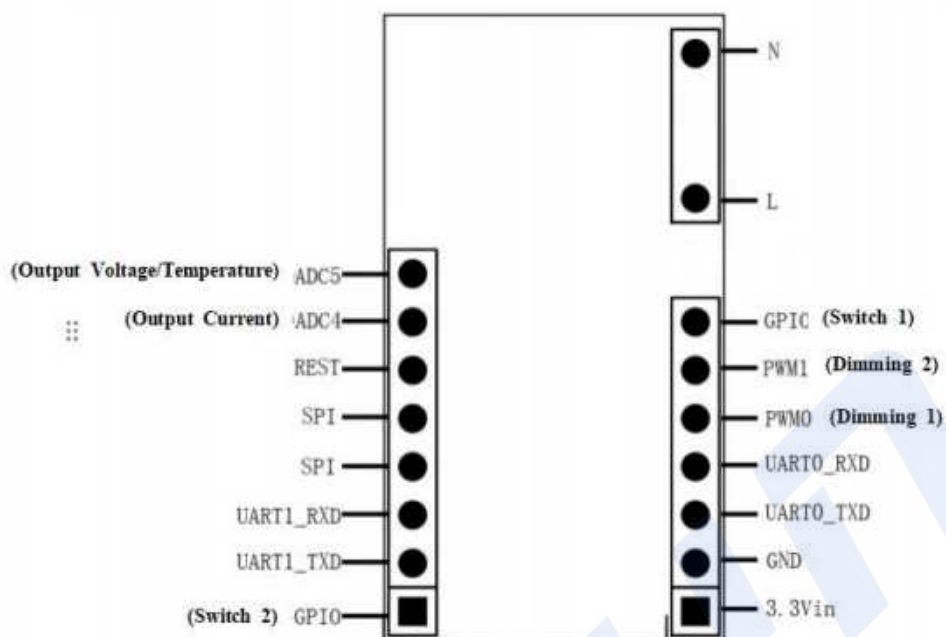
row)
Direct vertical PCB mounting for space-saving installations



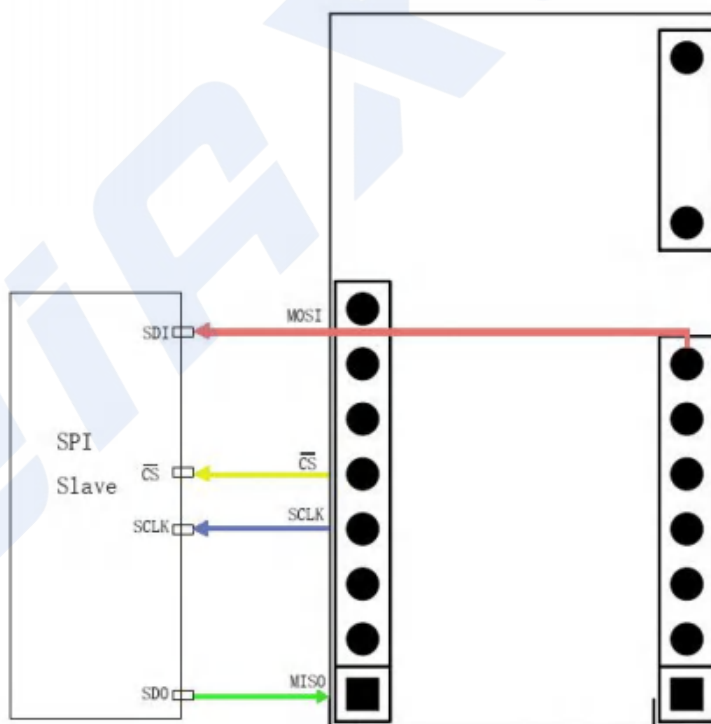
2) Dual-Port Interface Application Recommendation

Recommended Model: JMN-L80A-Z (180° straight pin header, dual-row)
row)



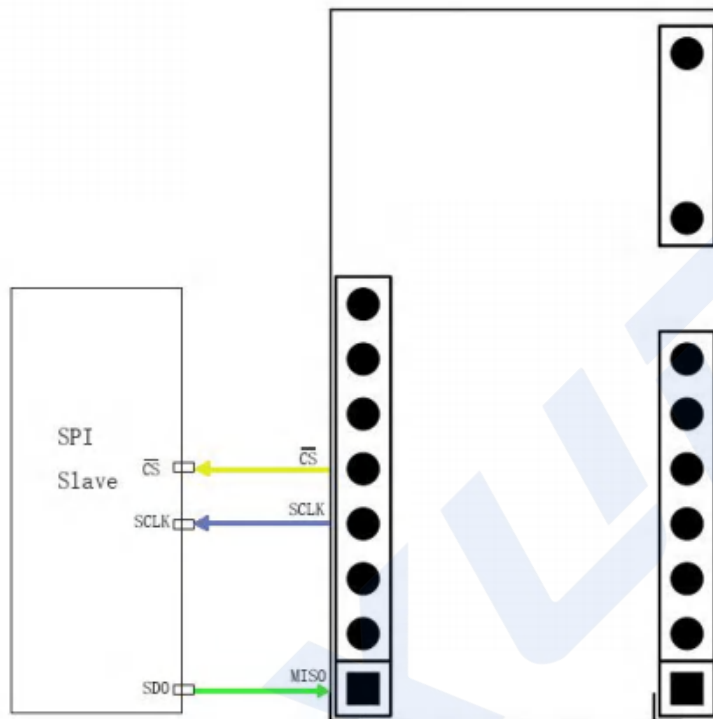


3) SPI Interface Application Recommendation (Four-wire System)



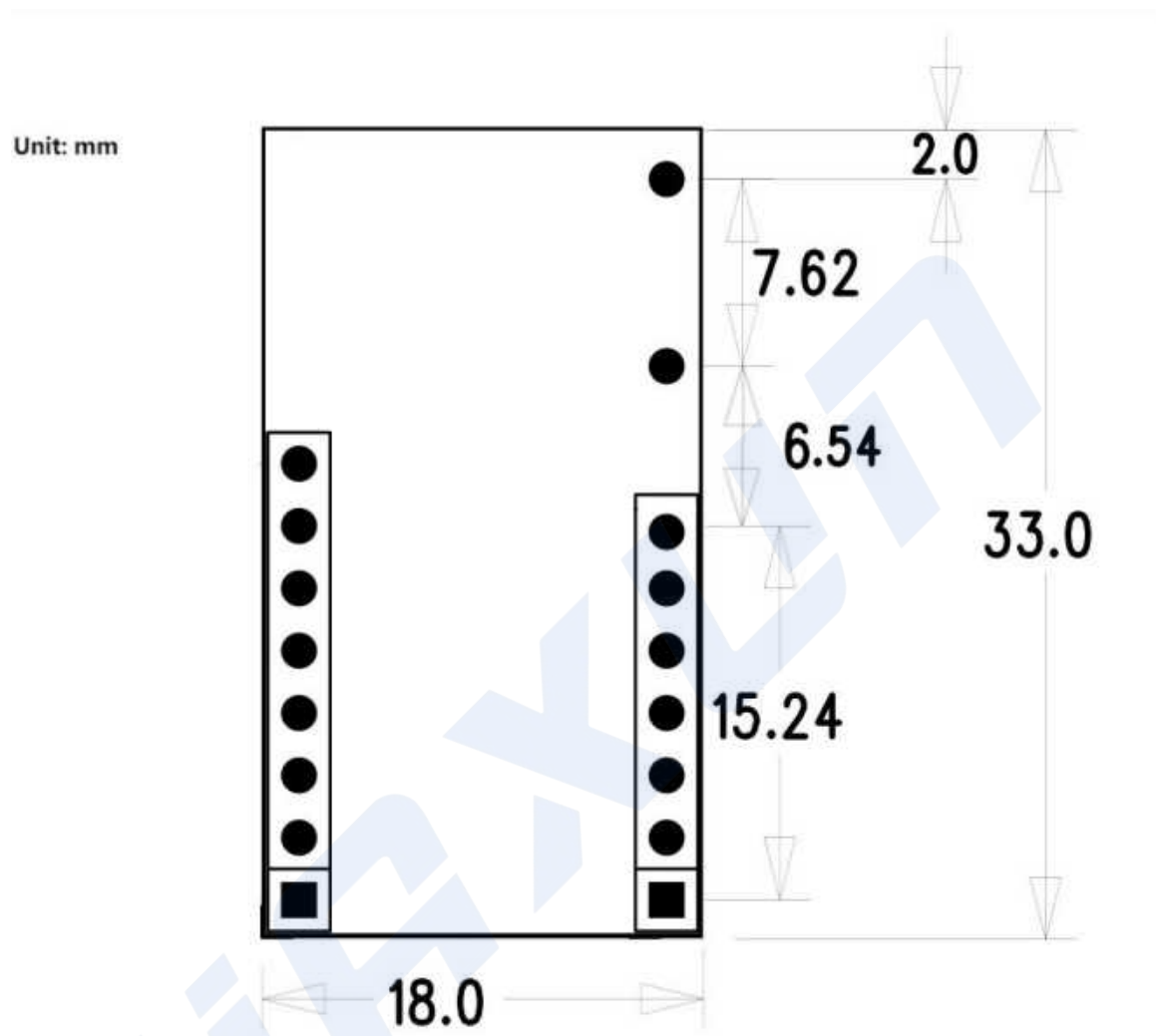
4) SPI Interface Application Recommendation (Three-wire System)

If the SPI Master needs to be used as MOSI, you can use software to configure pin 1 to use multiplexed signal 2 and configure it as SPI data output.

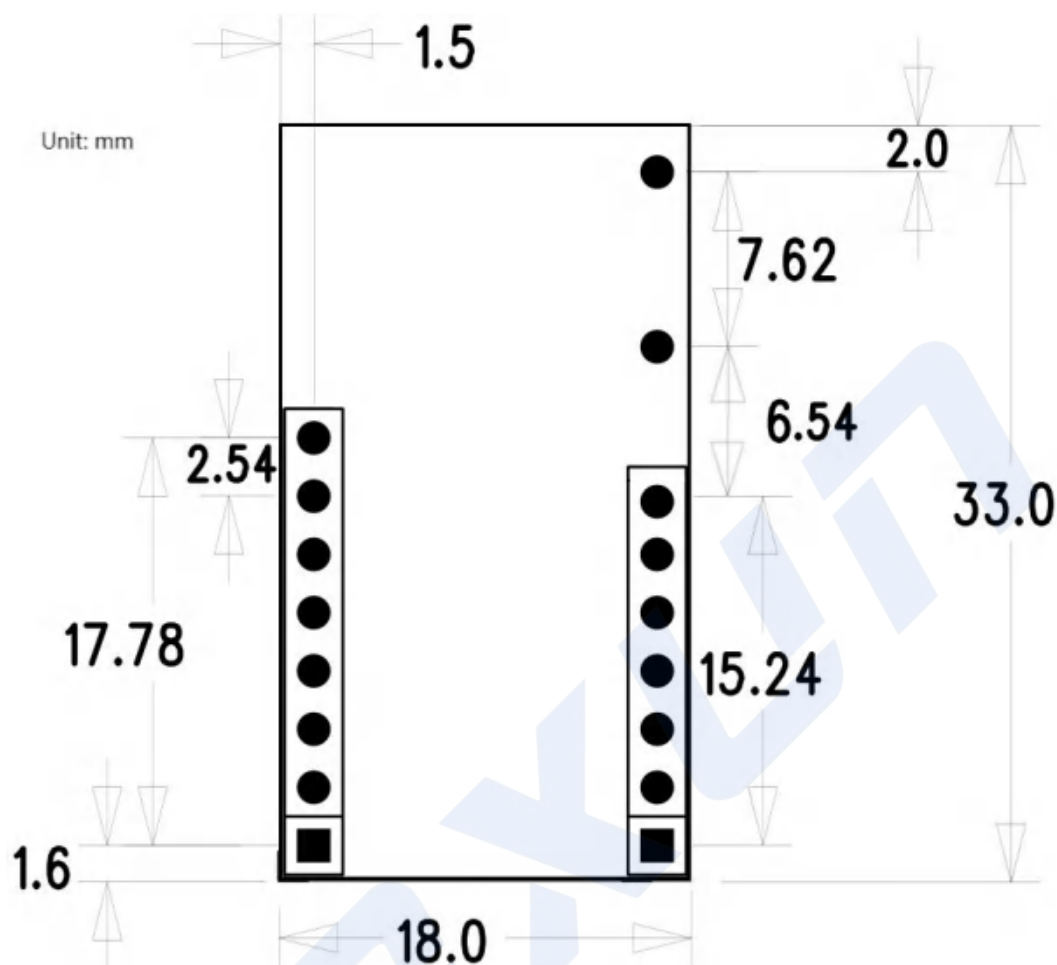


E. Module Package Size

1) 90° right-angle pin header, single-row



2) 180° straight pin header, dual-row



F. Hardware Design Description

1) Input Power Requirements

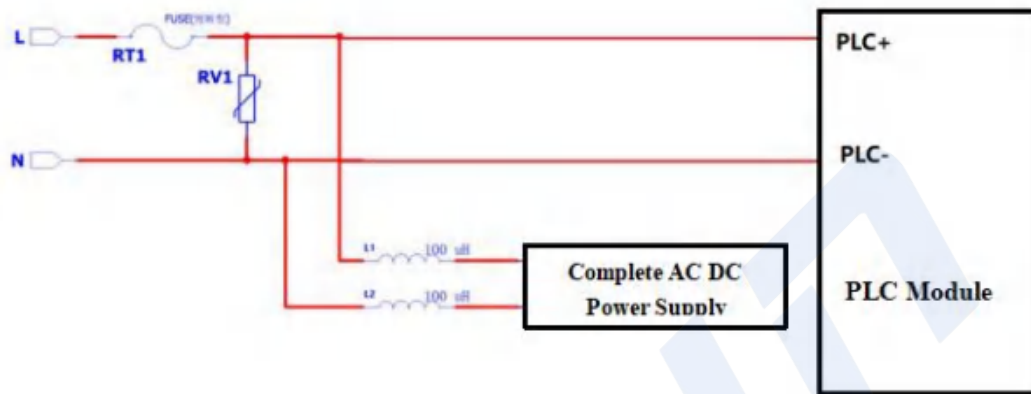
	Min	Typ	Max	Unit
3.3V _{in}	3.0	3.3	3.6	V

- Place at least one 10uF, 0.1uF ground energy storage capacitor near the 3.3V input of the module on the mainboard to reduce the power ripple. The peak-to-peak value of the ripple is within 100mV_{pp}.
- The module 3.3V is isolated from other 3.3V on the mainboard by using 600R/100MHz, 1A or more ferrite beads.
- The module 3.3V circuit guarantees at least 200mA or more current requirements.



2) PLC Signal Peripheral Design

For the overall product design, the safety protection design on the L/N line, and the PLC signal coupling design, it is strongly recommended to refer to the following circuit diagram and material selection.



Note: RT1 in the figure is a fuse. The PLC signal access point needs to be behind the varistor (RV1). The varistor junction capacitance is recommended to be less than 600pF. Two differential mode inductors (L1/L2) need to be connected in series behind the PLC signal to isolate it from the power supply of the whole machine. The differential mode inductor value is recommended to be 50~100uH.

Design Suggestions:

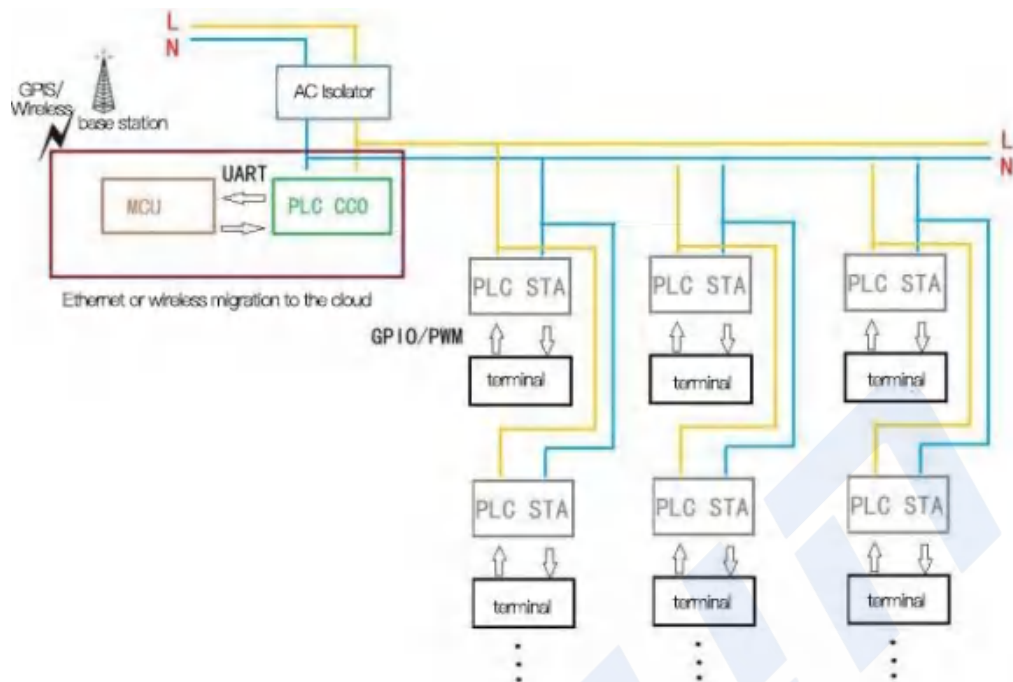
- The peak-to-peak ripple voltage on the 3.3V power rail must be maintained below 100mVpp to ensure optimal PLC performance.
- Compared with narrowband communication signals of several hundred kHz, broadband carrier communication has a wider bandwidth and higher frequency, which requires that there should be no large capacitors between the zero and live wires of the communication channel to reduce the attenuation of the communication signal. In the figure above, no capacitors exceeding 600pF are allowed in front of the differential mode inductor (if multiple devices are connected in parallel, the total capacitance of the parallel capacitors must be considered).



- If the whole machine needs to use X capacitors to reduce the differential noise on L-N, it is recommended to place the X capacitor after the 100uH inductor. In addition to reducing noise, it can also increase the impedance of the carrier channel and reduce the attenuation of the PLC signal. At the same time, the recommended capacitance is 2.2nF (the smaller the capacitance, the better). If you need to use a Y capacitor, please place it after the inductor (the smaller the capacitance of the Y capacitor, the better, but the impact of the Y capacitor on the PLC signal is less than that of the X capacitor).
- The switching frequency of the concentrator DCDC power supply is recommended to be lower than 1MHz to suppress out-of-band noise and limit the high-frequency out-of-band impact to less than 10dB, thereby reducing the risk of exceeding the EMI standard of the entire machine and reducing the impact on carrier communication.
- According to the protection level requirements of the whole machine, it is recommended to use a suitable varistor and fuse together, but the junction capacitance of the varistor is recommended to be as small as possible (the total L-N parallel capacitance does not exceed 600pF).
- The protection capability of the whole machine protection varistor should cover the PLC carrier circuit. The layout and wiring should ensure that the external power supply line passes through the varistor first, and then supplies power to the PLC carrier circuit and other circuits.
- When laying out the PCB, pay attention to the safety clearance requirements between the AC220 high-voltage terminal and the PLC module low-voltage terminal.
- The RX channel of the PLC carrier circuit, especially the filter and coupling coil parts, are also prone to absorbing space electromagnetic radiation interference, deteriorating the board noise floor and reducing the PLC receiving performance. Therefore, in the device layout, the interference source circuit, such as DCDC, is required to be far away from the sensitive circuit.



3) CCO and STA Typical Networking Diagram



- CCO is the PLC centralized controller, and STA is the PLC station.
- CCO and STA have the same hardware but different software.
- In simple applications, CCO can be networked independently without an external MCU. Networking that requires cloud access requires an external MCU to be implemented through wired Ethernet or wireless.
- In a typical CCO networking environment, it is recommended to add an AC220 isolator to the 220VAC line at the front end of the CCO to filter out noise from other power networks to avoid affecting the local CCO network communication quality. This also reduces the interference of the local CCO on other PLC communication networks.

G. Disclaimer

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